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DEVELOPMENT OF SINGLE CELL PROTECTORS FOR SEALED SILVER-ZINC CELLS

Phase I Final Report

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16 Abstract

The single cell protector (SCP) assembly capable of protecting a single silver-zinc (Ag Zn) battery cell was designed, fabricated, and tested. The SCP provides cell-level protection against overcharge and overdischarge by a bypass circuit. The bypass circuit consists of a magnetic-latching relay that is controlled by the high-and low-voltage limit comparators. Although designed specifically for secondary Ag-Zn cells, the SCP is flexible enough to be adapted to other rechargeable cells. Eighteen SCPs were used in life testing of an 18-cell battery. The cells were sealed Ag-Zn system with inorganic separators.

For comparison, another 18-cell battery was subjected to identical life test conditions, but with battery-level protection rather than cell-level. After 111 cycles of simulated synchronous orbit at 40% depth of discharge and a temperature of 22°C, no significant differences can be seen between cell-level and battery-level control. Cycle testing of two batteries will continue during the Phase II contract period (April 1976 to April 1977).

An alternative approach to the SCP design in the form of a microprocessor-based system was conceptually designed. A breadboard demonstration using an Intel 8008 microprocessor was also successfully conducted on a 10-cell silver-zinc battery pack. The comparison of SCP and microprocessor approaches is also presented and a preferred approach for Ag-Zn battery protection is discussed.

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FOREWORD

This report covers the work performed for the National Aeronautics and Space Administration (NASA), Lewis Research Center, during the Phase I period of contract NAS3-19432. The Phase I period was from April 1975 to April 1976. During the Phase II program, the life test program started in Phase I will continue until battery failure or the end of the contract period (April 1977), whichever occurs first.

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SUMMARY

The single cell protector (SCP) design capable of providing overcharge and overdischarge protection of a single silver-zince (Ag-Zn) cell was designed, fabricated, and tested. Eighteen SCPs were assembled and used in life cycle testing of an 18-cell battery pack. A single SCP is connected to an individual cell; and a relay is used to switch the cell into or out of a series-wired battery configuration. Principal elements in the SCP are the two upper and lower voltage limit comparators and a magnetic latching relay, which is used as the cell bypass device. The SCPs were also designed to be useful for other rechargeable cells, both sealed and unsealed, where voltage cutoff can be used as the criterion for charge or discharge termination. The cells are a sealed Ag-Zn system that uses inorganic fuel-cell grade asbestos separators.

The SCP was packaged to withstand the normal handling expected in a laboratory environment. To facilitate circuit repairs or part replacement, all internally mounted components were made readily accessible. Consistent with these criteria, fabrication cost and size of the SCP were kept to a minimum.

To determine the benefits of cell level protection, an 18-cell battery pack without cell-level control was also life tested. The two batteries were subjected to simulated synchronous (24-hour) orbit at 40% depth of discharge at 22°C. After 111 cycles during Phase I testing, no significant battery performance differences exist between the cell-level and battery-level protection approaches. It is significant that these two Ag-Zn battery packs have already operated an equivalent of at least 1 year in synchronous orbit with no apparent sign of impending failure. Life testing will continue during the Phase II period, April 1976 to April 1977.

An alternative approach to the SCP was investigated. This involved conceptual design of a microprocessor-based system capable of providing the same functions as the SCPs on an 18-cell battery. Comparative data were determined on cost, performance, reliability, power consumpation, and control flexibility. Also, a breadboard demonstration was successfully made using the Intel 8008 microprocessor. This demonstration involved cycling a 10-cell Ag-Zn battery under conditions identical to those for the two life-test batteries. The software was written in assembly language and loaded into the RAM via the ASR33 teletype. The evaluation of SCP versus microprocessor approaches has shown that, for laboratory application involving a large number of cells or batteries, the latter offers significant advantages in hardware cost, control flexibility, and data acquisition.

The SCPs are however more suitable for applications involving a limited number of cells or batteries with no major weight and volume constraints. Reason for this is primarily the simplicity in the SCP fabrication, attachment, and operation.

1.0 INTRODUCTION

In early 1972, NASA Lewis Research Center selected a cell-level control and protection system and developed a working prototype unit, referred to as the Solid State Voltage Comparator (SSVC). Martin Marietta was then contracted in 1975 to develop and fabricate a single cell protector (SCP) that introduced an improvement over the SSVC design. Two other major objectives of the program were to evaluate (1) cell-level and battery-level protection approaches by conducting a battery life test programand (2) an alternative approach to the SCP on cell-level protection based on use of a dedicated microprocessor. The cell-level protection was provided by the SCP.

In any secondary battery cell design, one of the most critical operations directly affecting the useful life of the cell is that of charging. Unlike the nickel-cadmium (Ni-Cd) cell, the sealed Ag-Zn cell cannot tolerate an appreciable overcharge. Thus, for these cells to operate properly as a battery pack, a suitable charge control system is necessary.

Under NASA Lewis Research Center sponshorship, Yardney Electric Corporation has developed a facility to fabricate sealed silver-zinc (Ag-Zn) cells (ref. 1 and 2). These cells have potentially longer cycle life than any of the other rechargable Ag-Zn cells with conventional separators. Their life capability is attributed primarily to the use of inorganic separator materials and secondarily to carefully controlled fabrication and processing conditions. Fifty of these cells were furnished by LeRC for use in verifying the SCP performance and in evaluating cell-level and battery-level protection approaches.

---

[1]I. C. Blake and C. Philip Donnel III: *Development and Fabrication of Sealed Silver Zinc Cells.* Yardney Electric Corporation, NASA CR-134591, Contract NAS3-16805, December 1973.

[2]C. Philip Donnel III: *Fabrication and Testing of Sealed AgZn Cells.* Yardney Electric Corporation, NASA CR-135048, June 1976.

2.0 TASK I - IMPROVED CELL PROTECTOR DEVELOPMENT

2.1 TASK OBJECTIVES

Objectives of Task I were to develop and fabricate improved cell protectors that provide cell-level protection. The scope of the task was defined by NASA LeRC as follows:

"The reference protector shall be the solid state voltage comparator (SSVC) unit developed by Lewis Research Center. The contractor shall evaluate the reference protector and develop an improved protector which is optimized as to compactness, cost, weight, power consumption and reliability. This improved protector shall be designed for attachment to, or incorporation in, a 40 ampere-hour Ag-Zn secondary cell. This unit must provide full protection against cell overcharge and overdischarge with the use of an appropriate by-pass circuit. Suitable terminals shall be provided for connecting said protected cells in a series string. The bypass and interconnecting circuitry shall be capable of switching and sustaining 20 amperes current.

"State of the art microelectronics shall be fully utilized wherever possible. Since the end product of Task I is to be utilized in Task II, design considerations shall be based on the requirements of both tasks."

Table 1 shows the test conditions for the Task II cycle test.

TABLE 1 TEST CONDITIONS FOR CYCLE TEST IN TASK II

Duration:		
Cycle	-	24 h
Charge	-	22.8 h
Discharge	-	1.2 h
Charge rate	-	0.75 A
Discharge rate	-	13.3 A.
Temperature	-	22°C

2.2 DEFINITION OF SILVER-ZINC CHARGE CONTROL METHOD

One of the most critical operations that can be performed on a cell, and one that most directly affects the useful life of the cell, is charging. One of the primary functions of a charge control system for any sealed secondary battery is to prevent the rupture of any battery cell from excessive pressure buildup during charge. This failure

mode is usually due to excessive overcharging.

Unlike the nickel-cadmium (Ni-Cd) cell, the silver-zinc (Ag-Zn) cell cannot tolerate appreciable overcharge because of less ability for oxygen recombination. Therefore, a proper termination of charging is much more critical on the Ag-Zn cell.

The two key criteria for the Ag-Zn cell charge control system are (1) overcharge must be terminated to limit the internal cell pressure to an acceptable level; (2) undercharging must be prevented to avoid depleting the battery energy during each successive cycle, which leads to battery failure. Therefore, empirical data characterizing the voltage/pressure profile under the basic operating conditions are necessary to define adequate charge control limits for the electronics.

It is a usual practice to define the charge control setting based on data obtained on a new cell. To ensure protection over the cycle life of the cell, it is also highly desirable to empirically determine the effects of aging (i.e, cycling). However, due to limited time available, the approach used in defining the charge control limits for the 40-Ah Ag-Zn cell was to characterize and use the data from the new cell. Furthermore, the effects of cycling on the internal pressure were determined under actual cycling conditions on two pressure-instrumented cells (see section 3.5.4, Group III Battery/ACDAS Test).

Basic guidelines used in obtaining the cell charging characteristics were:

1) Constant current charge mode was to be used. The cycle test to be conducted in Task II was to be 0.75 A charge rate with upper voltage limit.

2) Ambient chamber temperature of 22°C.

3) Cycling regime

    24-h orbit
    22.8-h day duration
    1.2-h night duration

To allow for the possible use of other charge rates and operating temperatures, parametric data were obtained at the following conditions:

Charge rates: 0.75, 1.5, 4.0, and 8.0A
Temperature: 10, 20, and 30°C.

Figures 1 thru 4 show the voltage and pressure profiles for the four charge rates, respectively. From these data, the cell

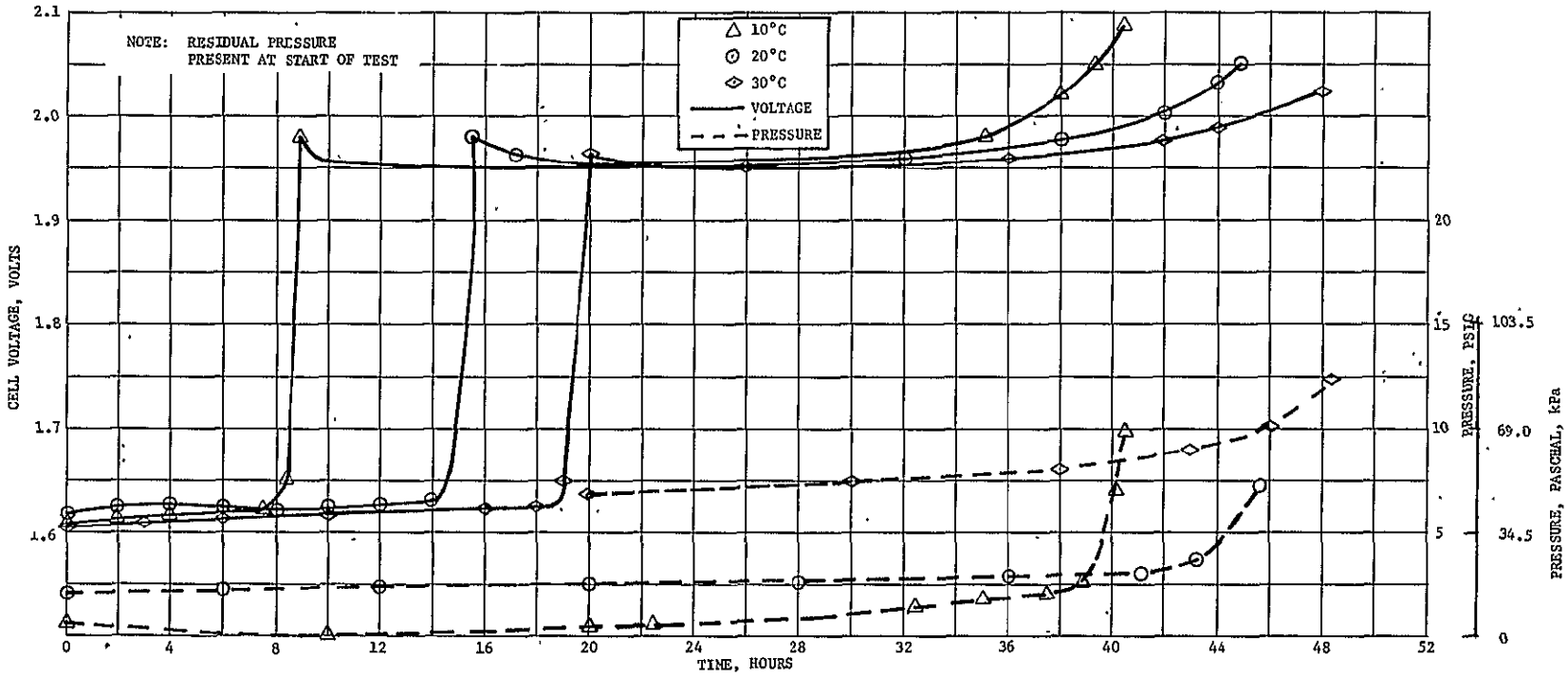


FIGURE 1 CHARGE VOLTAGE AND PRESSURE PROFILE AT 0.75-A RATE

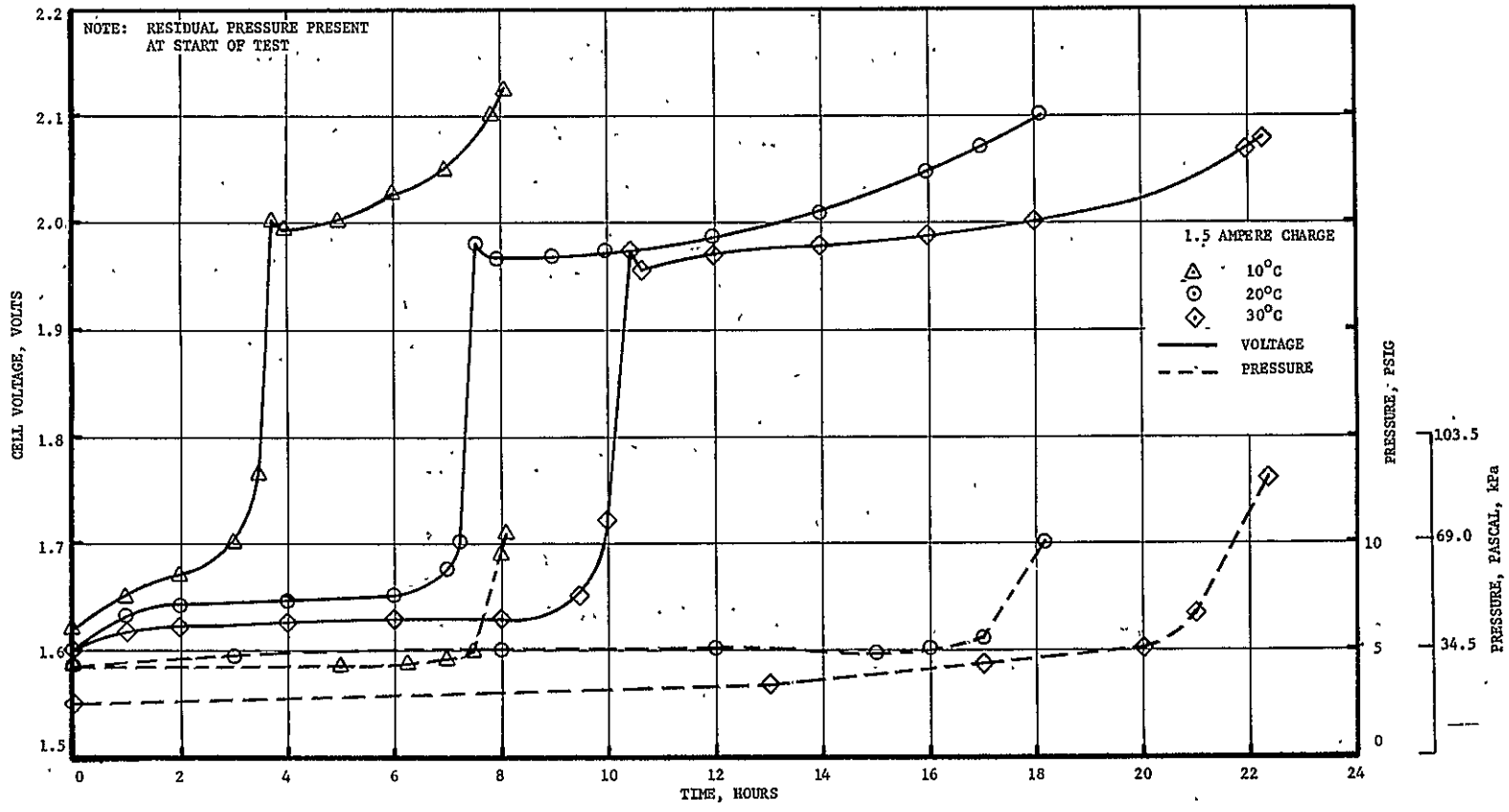


FIGURE 2 CHARGE VOLTAGE AND PRESSURE PROFILE AT 1.5-A RATE

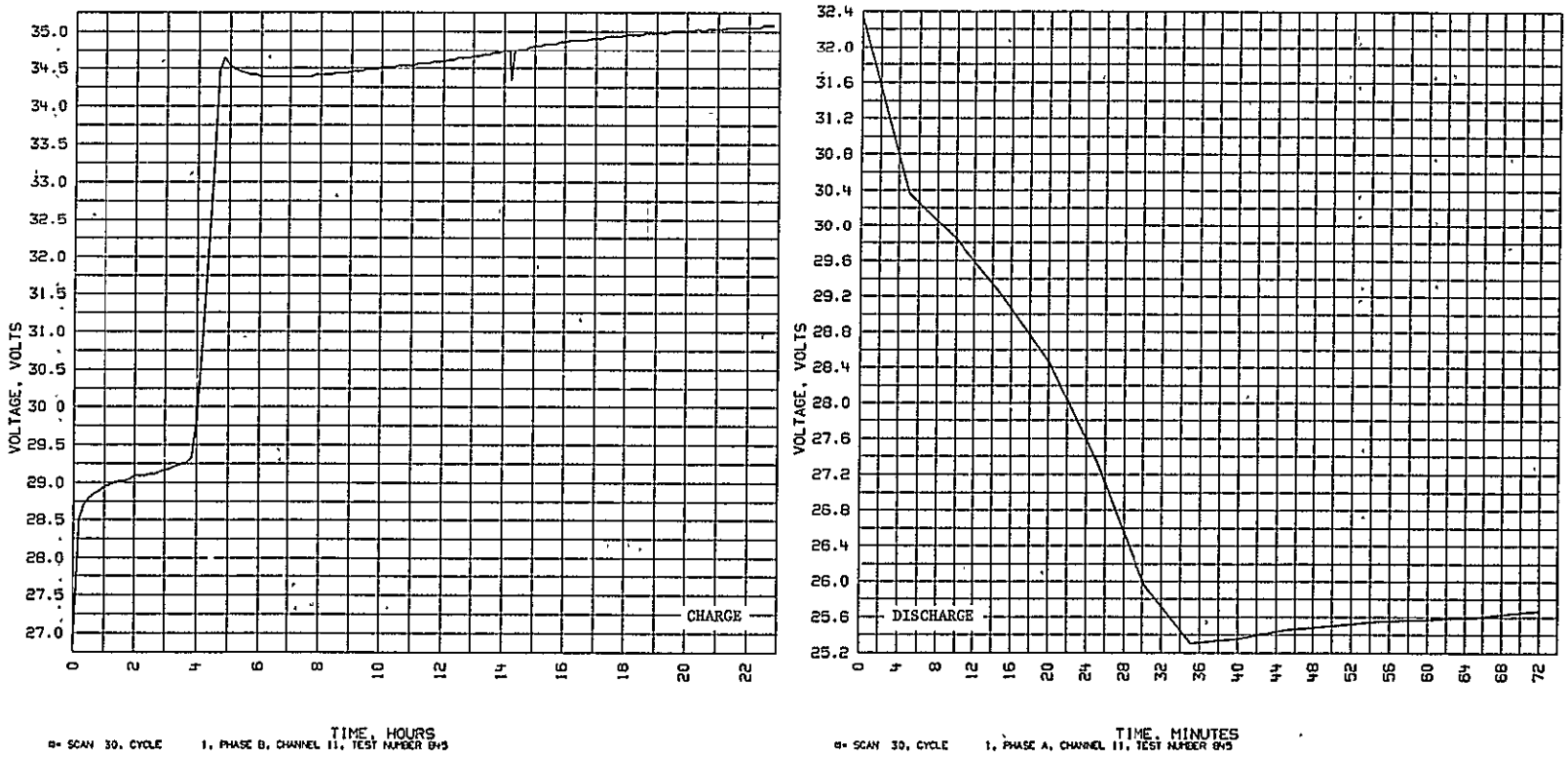


FIGURE 3 CHARGE VOLTAGE AND PRESSURE PROFILE AT 4.0-A RATE

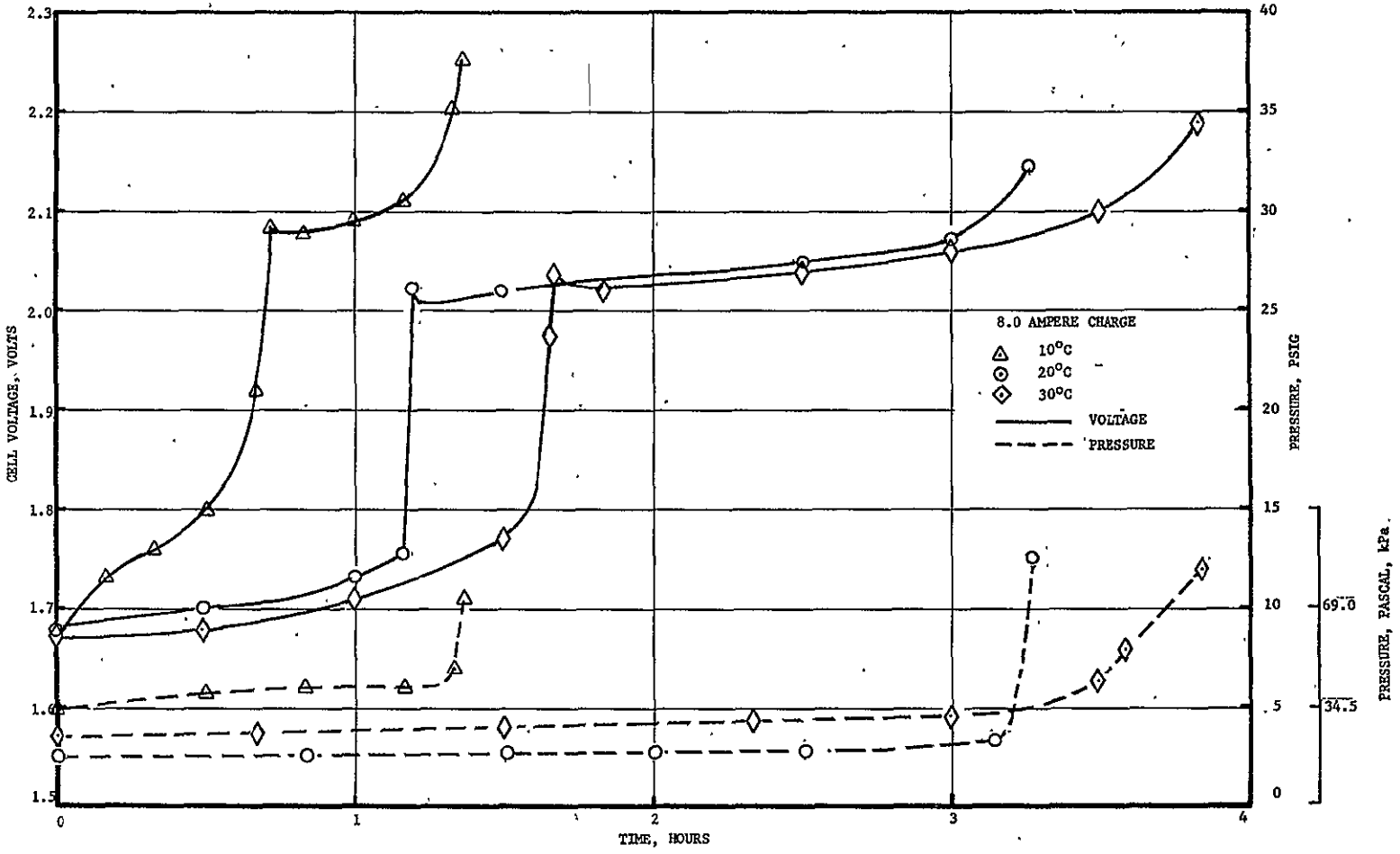


FIGURE 4 CHARGE VOLTAGE AND PRESSURE PROFILE AT 8-A RATE

voltage at the onset of O_2 pressure buildup (figure 5) and the rate of pressure rise (figure 6) as functions of charge rate were determined. Figure 5 shows that the charge voltage limit to avoid internal pressure buildup increases with increasing charge rate. Figure 6 indicates that the rate of pressure buildup is proportional to the overcharge current and decreases with increasing temperature.

Figure 7 shows the maximum cell pressure obtained during cycling at several charge voltage limits. These data show that a 2.0-Vdc cutoff is adequate to prevent pressure buildup at 0.75-A-charge rate.

Limited tests were conducted to determine the recombination rate under discharge and open-circuit conditions. Figures 8 and 9 are plots of cell voltage and pressure after a 0.75- and 8-A charge, respectively. In these tests, the cell was intentionally charged until pressure developed in the cell. The data clearly indicated that (1) pressure increases slightly during discharge,,(2) there is some gas recombination during open circuit stand; but the decay rate is too slow and cannot be depended on to effectively reduce the internal cell pressure in successiv 24-hour cycling.

The most significant result of the pressure evaluation is that any overcharge resulting in internal pressure buildup must be prevented. This can be done by properly terminating the charge at the empirically determined cutoff voltage. At a charge rate of 0.75 A at 22°C, this cutoff voltage should not exceed 2.0 Vdc.

Another characteristic of the Ag-Zn cell that was evaluated is the voltage surge (or spike) during the transition from the monoxide to the peroxide region (figure 10). This voltage spike can exceed the end-of-charge voltage cutoff limit for a short time. Thus, a major problem* in the SCP design was to allow the cell to continue charging past the voltage spike, yet terminate charging when the cell voltage reached the predetermined safe charge voltage limit.

Figure 11 shows the cell voltage profile at the 0.75-A rate around the monoxide-to-peroxide transition region. The plot shows that the peak voltage did not exceed 2.0 Vdc at 22°C. However, the design approach selected for the SCP was to assume that the voltage spike can exceed 2.0 Vdc at other temperatures or from aging, and to provide a necessary time delay at 1.75 Vdc up to 20 min before the desired cutoff voltage trip is enabled.

*Note that this problem is peculiar only to the constant current mode of charging compared to the constant voltage mode.

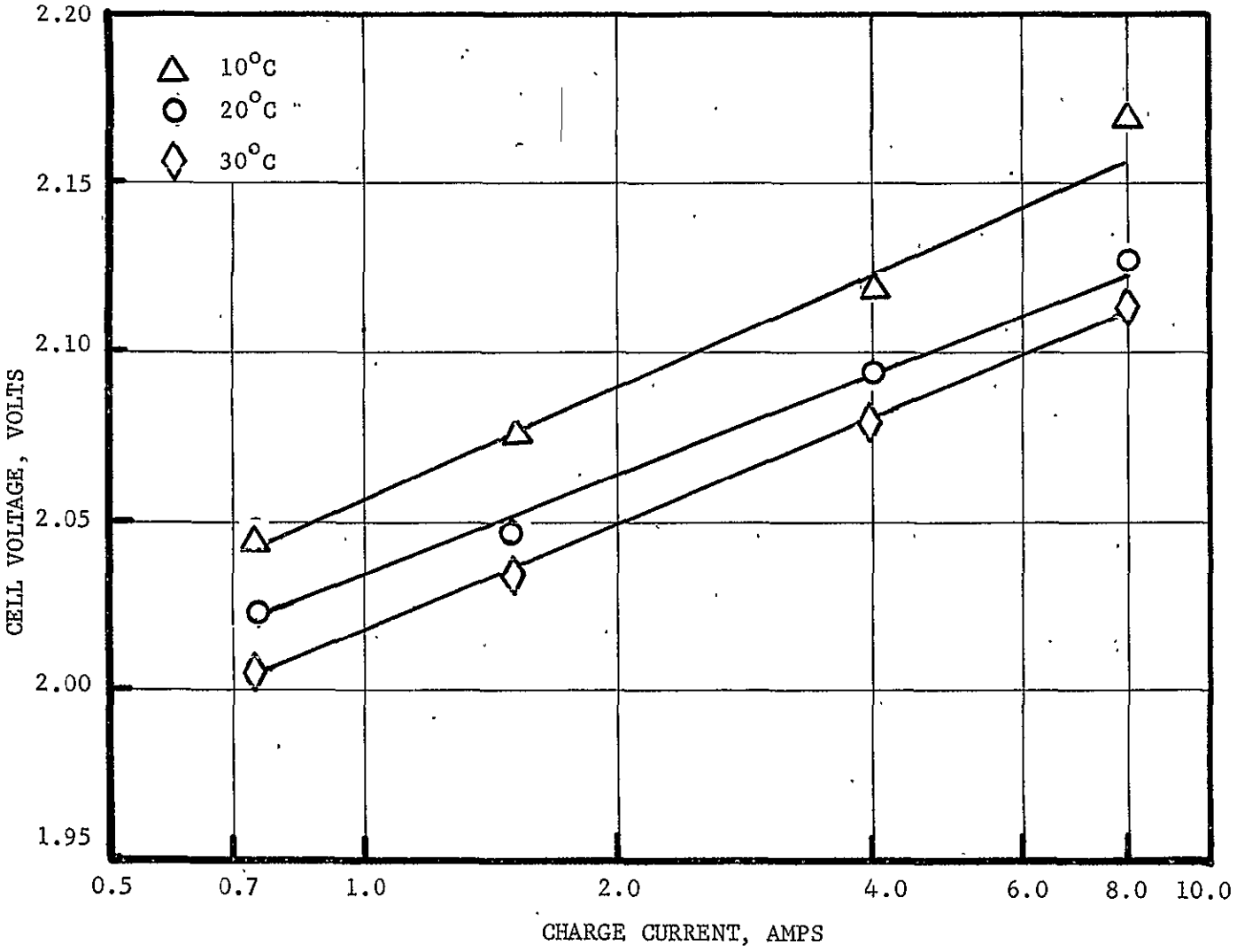


FIGURE 5. CELL VOLTAGE AT ONSET OF O_2 PRESSURE AS A FUNCTION OF OVERCHARGE CURRENT

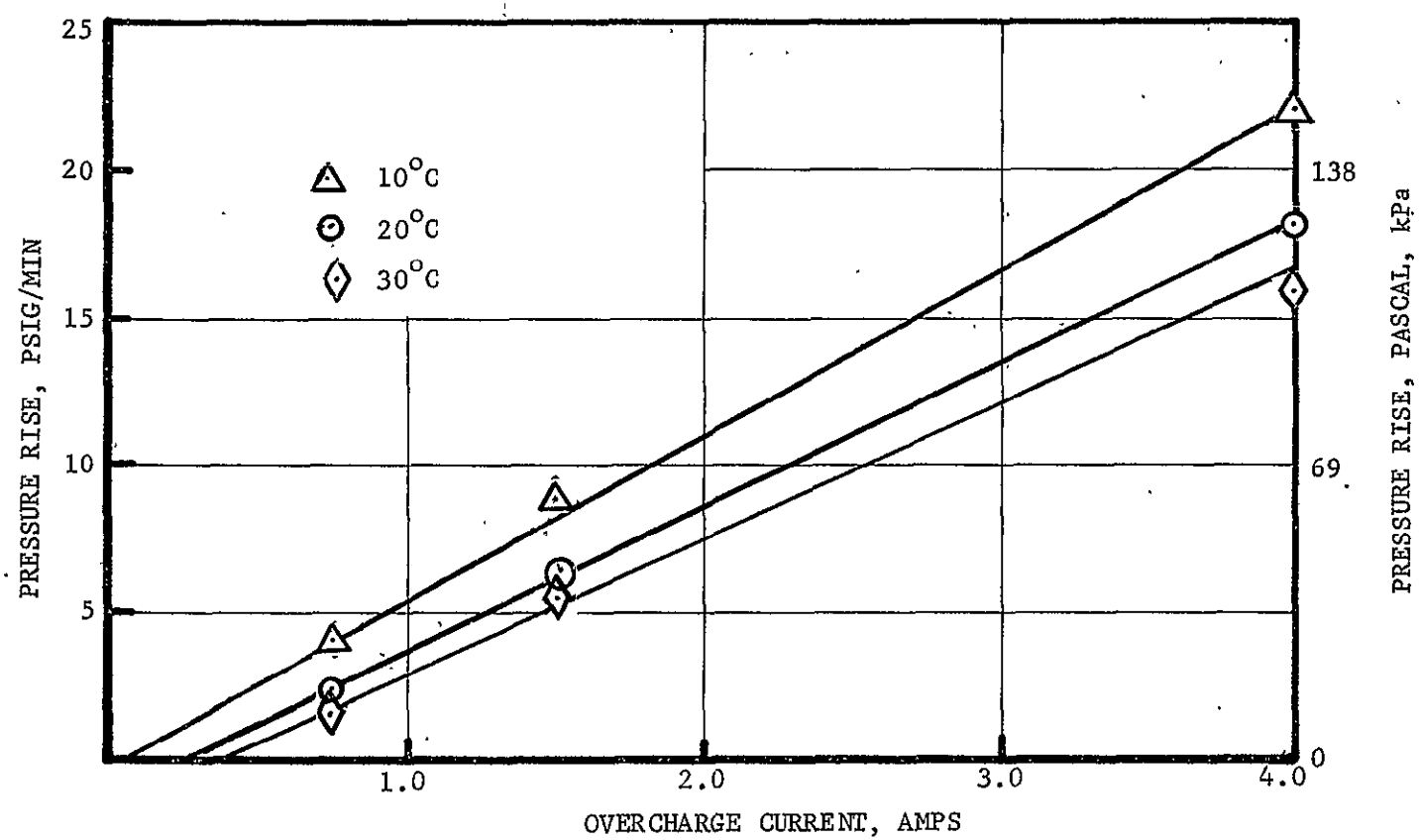


FIGURE 6. RATE OF PRESSURE RISE VS OVERCHARGE CURRENT

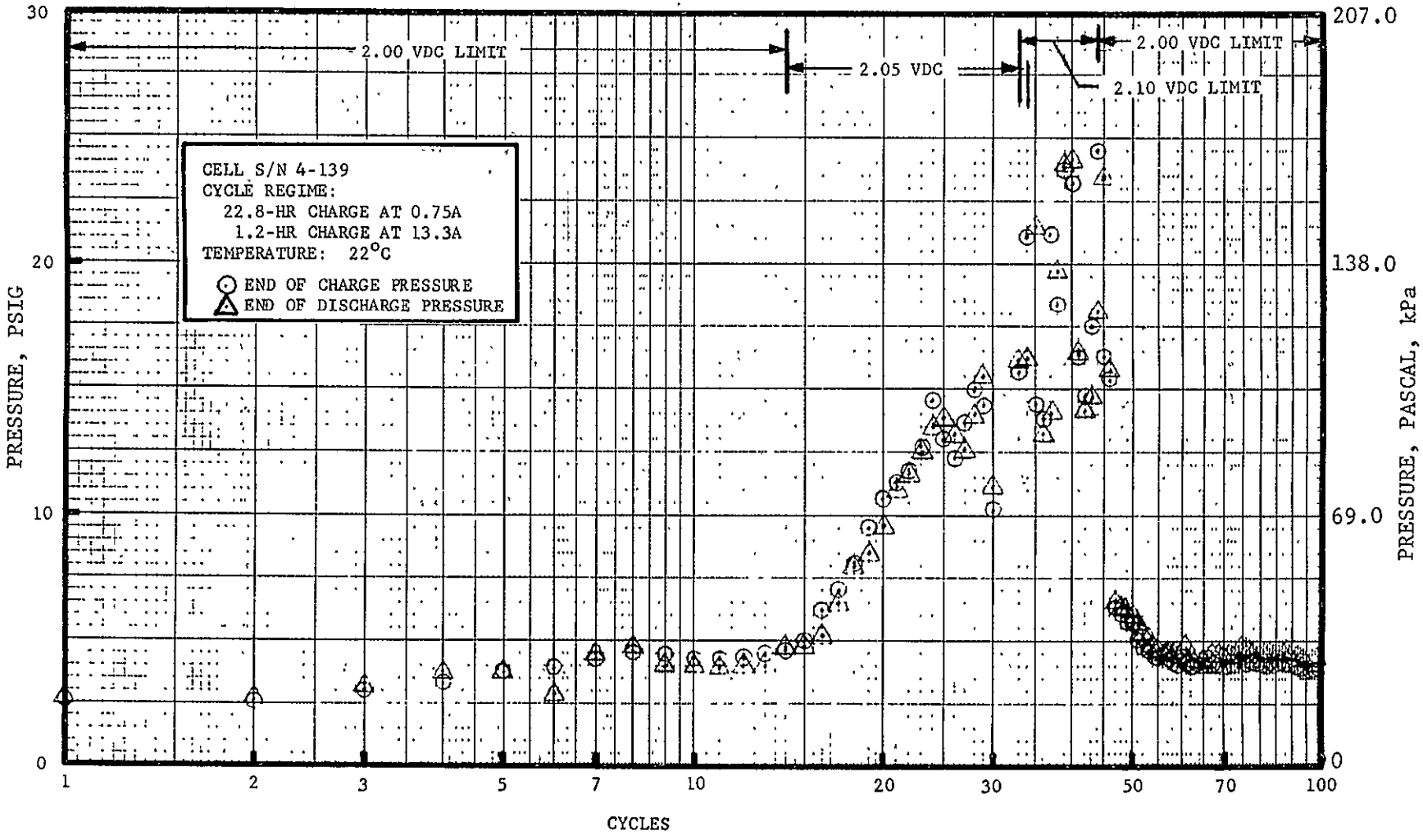


FIGURE 7 EFFECTS OF CHARGE VOLTAGE LIMIT ON INTERNAL CELL PRESSURE DURING CYCLING

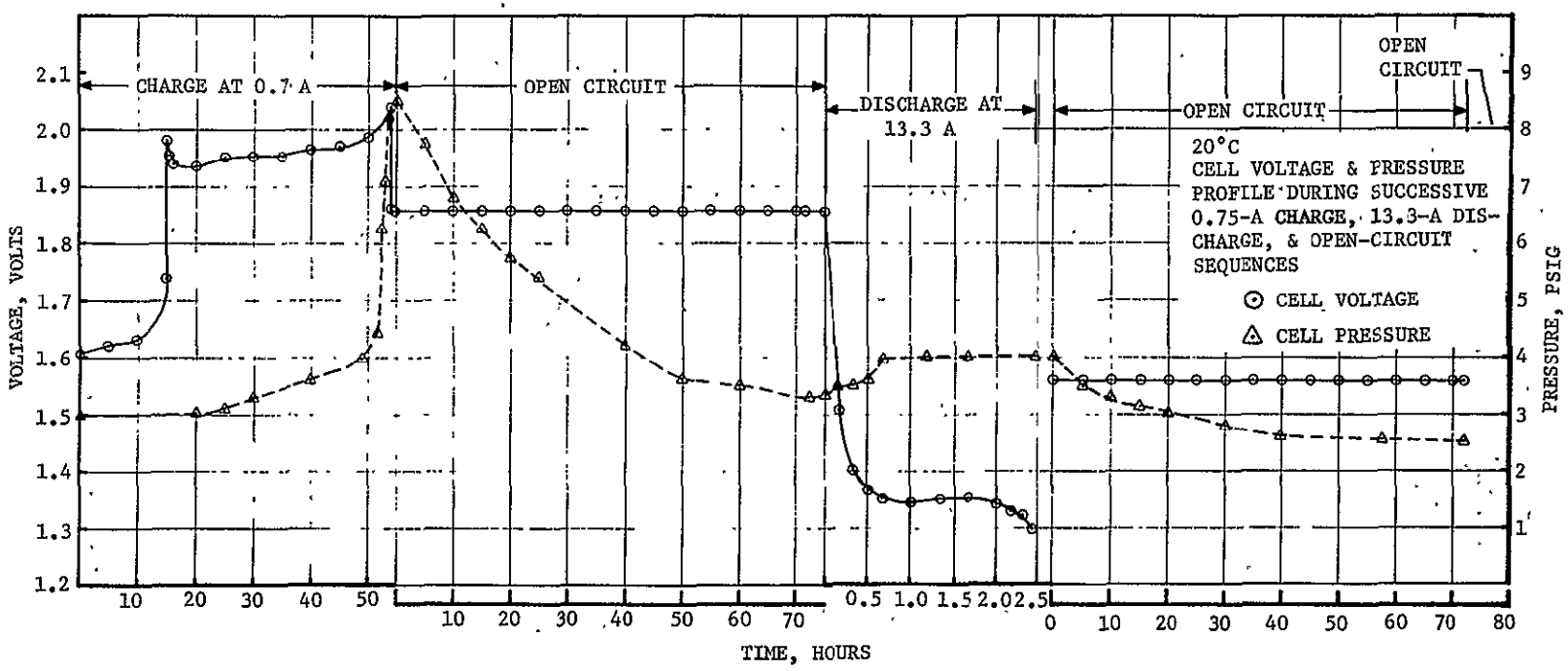


FIGURE 8. CELL VOLTAGE AND PRESSURE PROFILE DURING SUCCESSIVE 0.75-A CHARGE, 13.3-A DISCHARGE, AND OPEN-CIRCUIT SEQUENCES

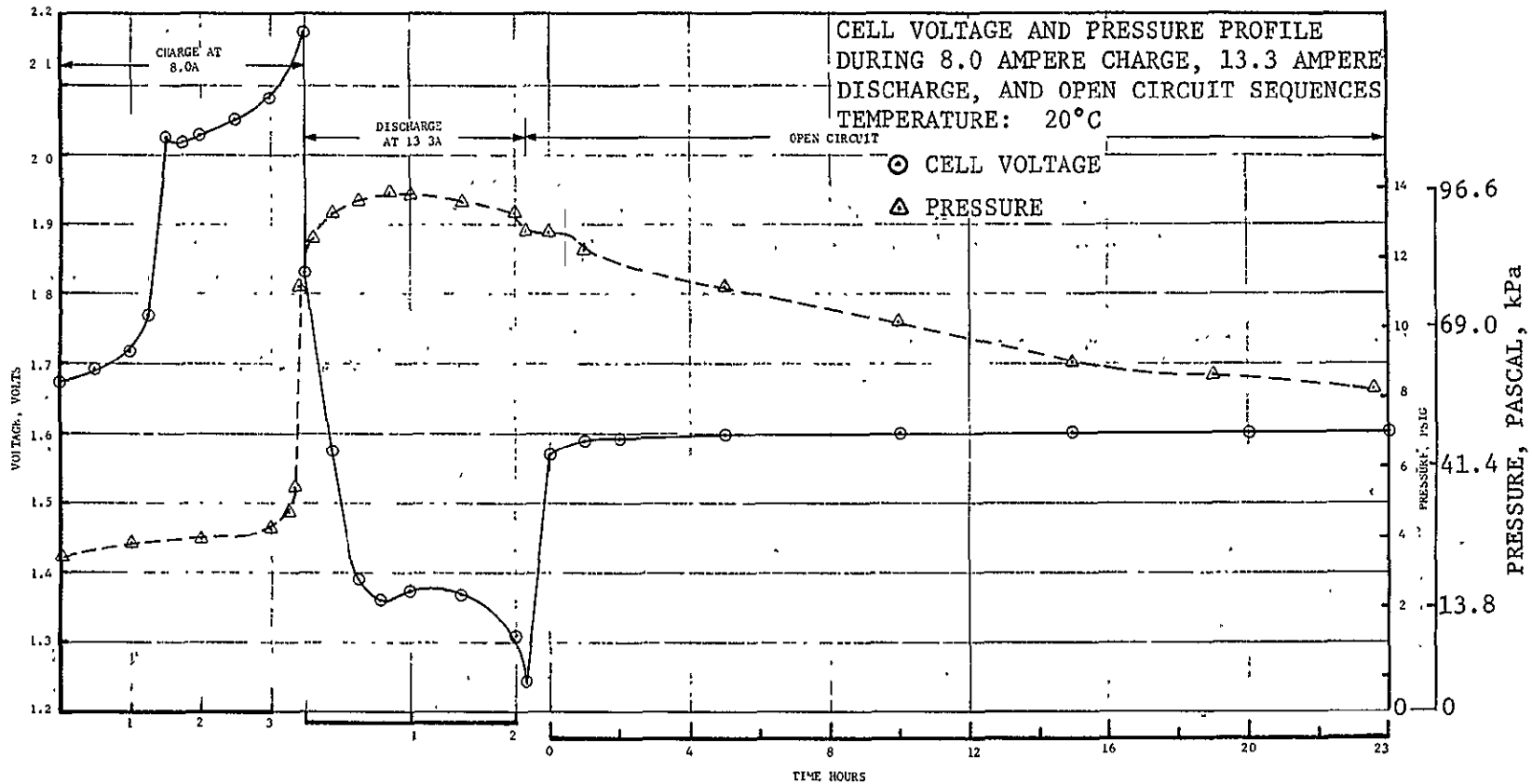


FIGURE 9 CELL VOLTAGE AND PRESSURE PROFILE DURING SUCCESSIVE 8.0-A CHARGE, 13.3-A DISCHARGE, AND OPEN-CIRCUIT SEQUENCES

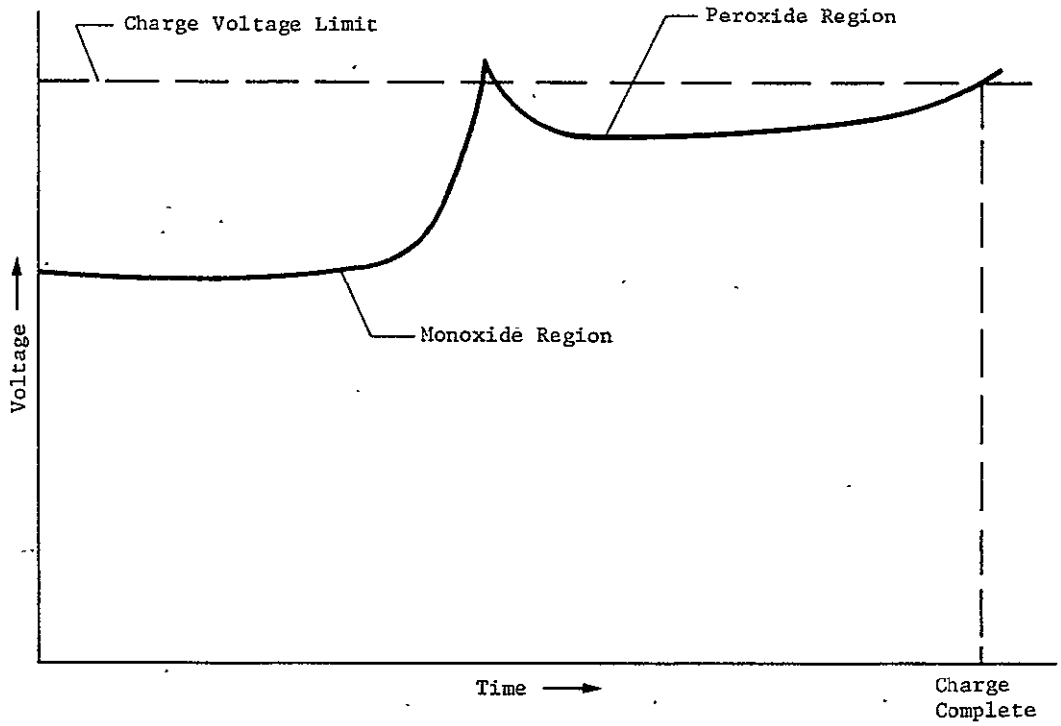


FIGURE 10 CHARGING CHARACTERISTICS OF AG-ZN CELL

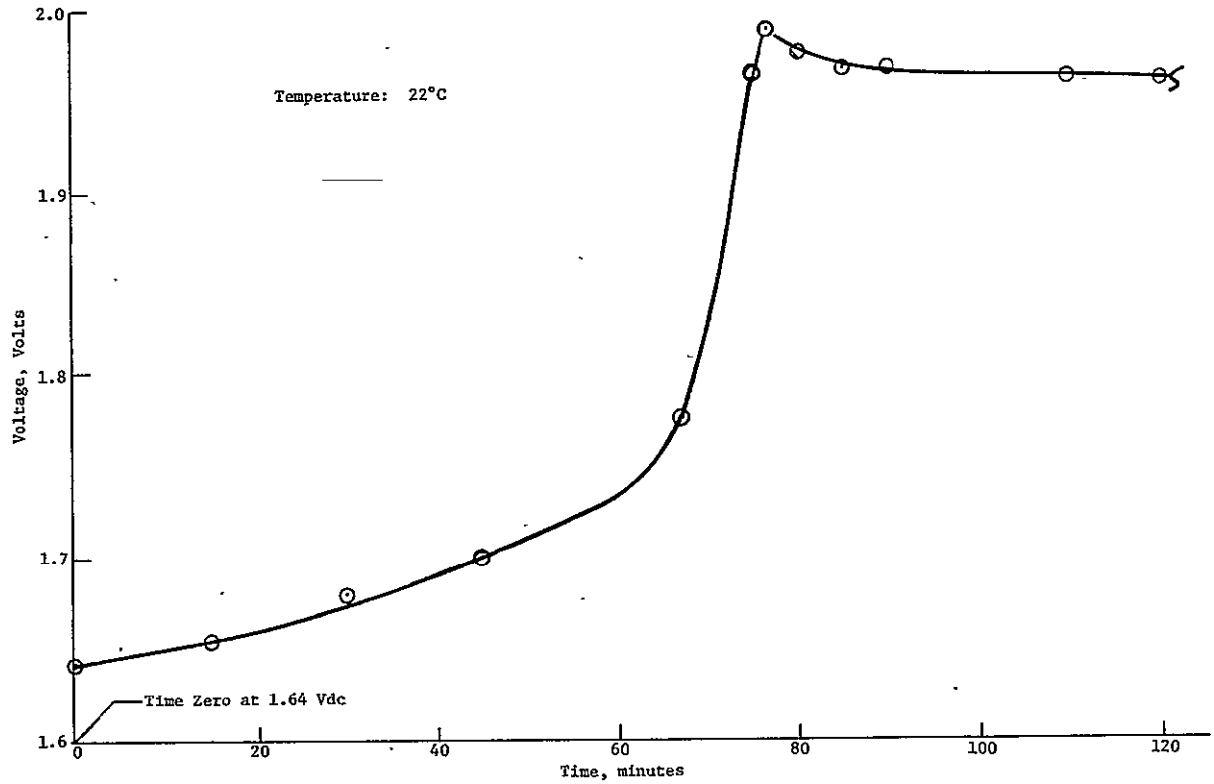


FIGURE 11 CELL VOLTAGE PROFILE AT 0.75-A CHARGE ILLUSTRATING MONOXIDE-PEROXIDE TRANSITION REGION

2.3 REFERENCE PROTECTOR--SOLID-STATE VOLTAGE COMPARATOR (SSVC)

Figure 12 is a block diagram of the SSVC, which is used as a basis of comparison for the SCP design. The SSVC uses a differential amplifier to sense the voltage of an individual cell in a series-wired battery string. The output of the differential amplifier is then applied to high-limit and low-limit comparators. The comparator outputs are OR-ed together to trigger a 0- to 4-minute adjustable one-shot circuit. This circuit controls a transistor driver that energizes a relay to remove the cell from the battery circuit. The cell can only be held out of circuit for the time corresponding to the time delay (4-min maximum) of the one-shot circuit. After this delay, the cell will return to circuit and, if the comparators again sense an out-of-limit condition, the one-shot circuit will be triggered and the cell again removed from circuit. Operation of the circuit for a cell in overcharge or overdischarge is thus a pulsing operation. The cell is held out of circuit for the time delay of the one-shot circuit, then momentarily switched back into circuit before being switched out again. An alternative latching mode of operation can be obtained by using a spare set of relay contacts to keep the coil energized after being triggered. This mode is obtained in the existing design by placing switch S1 on the instrument panel in figure 12 to the LATCH position. The RESET pushbutton switch must then be pushed to return a cell to the circuit.

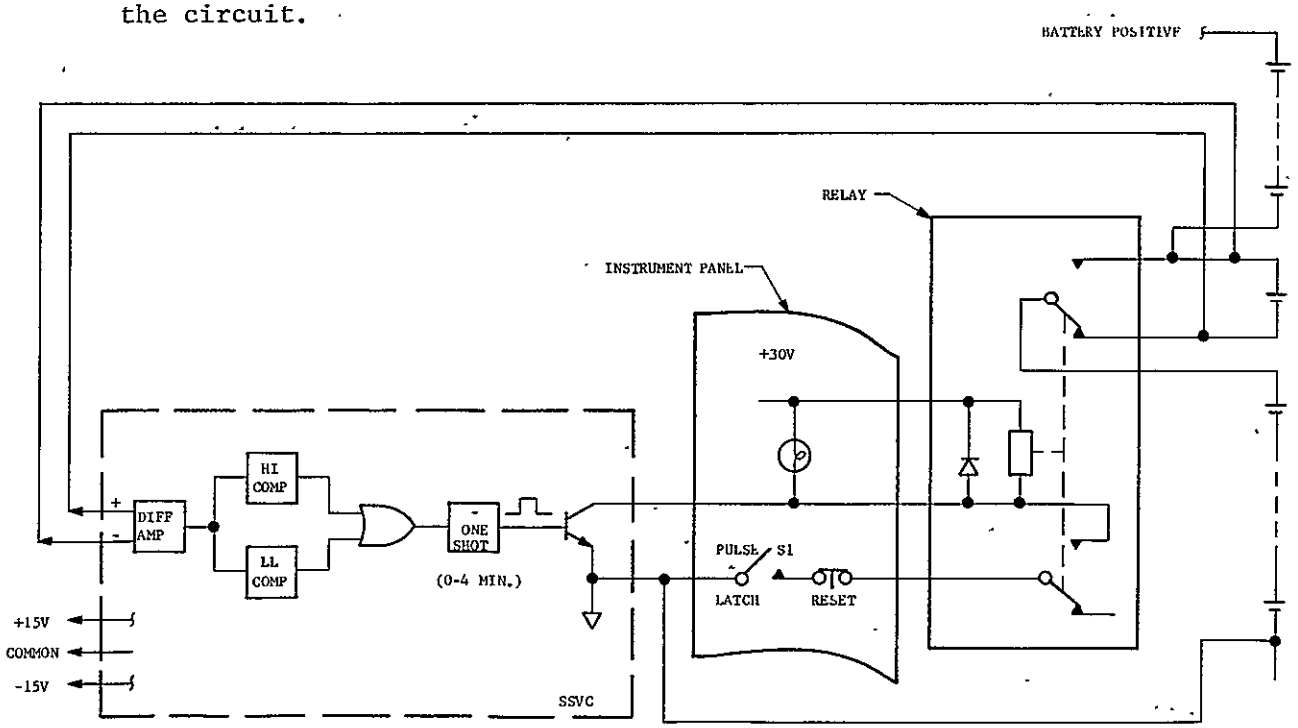


FIGURE 12 EXISTING SSVC DESIGN

The evaluation of the SSVC design revealed several areas that can be improved upon. These are:

1) Voltage Spike - The charge voltage spike characteristic of Ag-Zn cells causes the SSVC to terminate charging prematurely. If the SSVC is in the pulsing mode of operation, the cell will eventually "bump" its way over the spike and finish charging. However, this leads to an uncertainty in the charge termination point and is undersirable.

2) Power Consumption - The SSVC consumes considerable power, primarily in the relay. The standby power consumption with the cell in circuit is estimated to be 0.43 W. With the cell out of circuit, the power consumption is estimated to be 3.3 W. For an 18-cell battery using a single SSVC protector for each cell, the power consumption for the cell-out condition becomes undesirably large (59.4 W).

3) Number of Power Supplies - Three power supplies are required for SSVC operation: $\pm$ 15 Vdc for the detector and control circuitry and +30 Vdc for relay coil power. It is desirable to reduce the number of power supplies required.

4) Bus Voltage Interruption - During discharge, when a cell is switched out of circuit, the bus voltage is interrupted during the relay contact transition time. This is undesirable in a power system configuration with only one battery.

5) Sensitive Circuitry - During charging, when a cell is switched out of-circuit and the bus is interrupted, the charging source can put a large enough transient voltage on the bus to damage the differential amplifiers in the SSVCs.

6) Packaging - SSVC detection and control circuits are assembled on individual circuit cards, one card for each SSVC. The cards required for a battery of cells are then mounted together in an instrument panel assembly. The result is that the SSVCs are remote from the cells and from the cell bypass relays. This packaging arrangement is in some cases undesirable because of the complexity involved and noise susceptibility or noise generated due to long leads. A modular protector design containing the detection and control circuitry and bypass relay in one package and mounted close to the cell being protected is considered desirable.

7) Common Mode Range - SSVC implementation is constrained to operate with batteries whose maximum voltage is less than 24 V. This

constraint is due to the common mode limitations of the differential amplifier, which can operate only if the voltage at the differential amplifier inputs is held to less than 24 V. A means of using the SSVCs with battery voltages in excess of 24 Vdc is shown in figure 13. Here the SSVC reference is at the midpoint of the battery and the differential amplifier input is between +24 and -24 Vdc. This is an acceptable mode of operation only if the detector has a floating ground. A photocoupler is used to interface the floating detector and control circuitry to the relay driver circuitry.

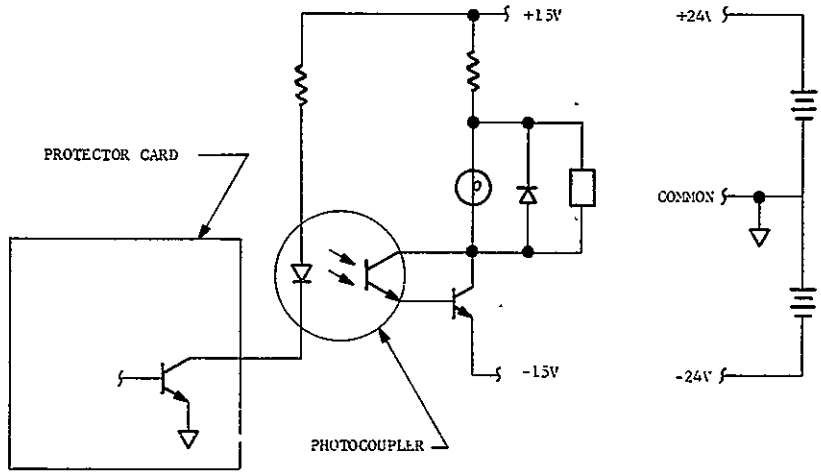


FIGURE 13 SSVC HIGH-VOLTAGE IMPLEMENTATION

8) Common Mode Sensitivity - Accurate measurement of a relatively small cell voltage superimposed on a large common mode voltage is a difficult circuit design problem. A conventional method of obtaining this measurement, and the method used in the SSVC, is to use a differential amplifier, as shown in figure 14. However, the differential amplifier is severely handicapped by error sensitivity coefficients for the four feedback resistors R1, R2, R3, and R4, which produce an error in the output voltage that is amplified out of proportion to the resistor error source. This error amplification effect is caused by the presence of the common mode battery voltage, V_{CM}. If, for illustration, the operational amplifier in figure 14 is assumed to be ideal, the amplifier output is described by,

$$V_o = \frac{R_3}{R_1}\left[\frac{R_4}{R_3}\left(\frac{R_1 + R_3}{R_2 + R_4}\right) V_2 - V_1\right] \qquad [1]$$

For proper circuit operation, the resistors are matched so that R1 = R2 and R3 = R4. Equation [1] then reduces to

$$V_o = \frac{R_3}{R_1} (V_2 - V_1)$$

or

$$V_o = - \frac{R_3}{R_1} V_X \qquad [2]$$

Equation [2] represents the desired output. The signal V_o is proportional to the differential input V_X and independent of the common mode voltage, V_{CM}. To obtain this desirable characteristic in the circuit, the resistors must be well matched.

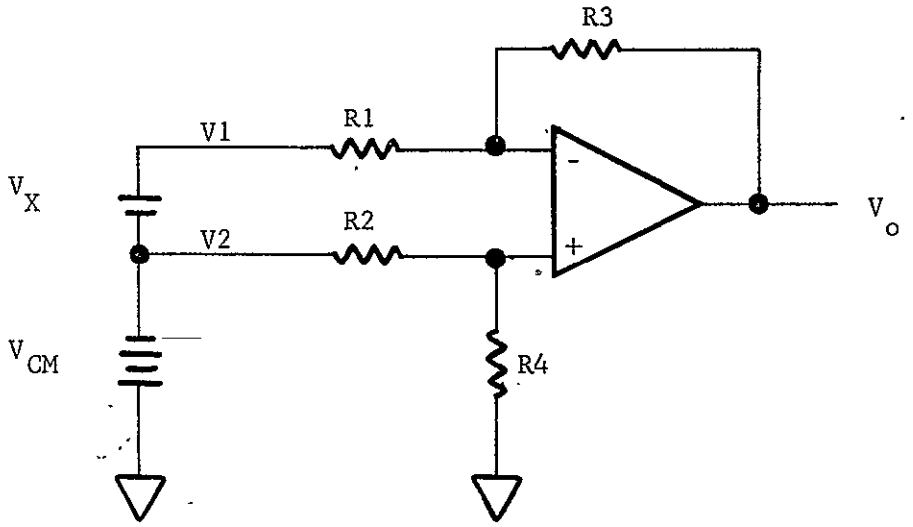


FIGURE 2.3-3 DIFFERENTIAL AMPLIFIER

The effect of resistor parameter variations on circuit operation can be seen by letting $V_1 = V_2 = V_{CM}$ in equation [1] and combining terms. We then have

$$V_o = \left[\frac{1 - \left(\frac{R_3}{R_1}\right)\left(\frac{R_2}{R_4}\right)}{1 + \frac{R_2}{R_4}} \right] V_{CM} \qquad [3]$$

With matched resistors; the numerator in equation [3] vanishes and V_o is independent of V_{CM}. However, if the resistors are slightly mismatched, an error is obtained in V_o, the magnitude of which is proportional to V_{CM}. Defining a resistor sensitivity coefficient S_x, as the change in V_o (normalized to full-scale output) to a fractional resistance change in R_x, we have

$$S_x = \frac{V_o/V_o(FS)}{R_x/R_x} = \frac{R_x}{V_o}\frac{\partial V_o}{\partial R_x} \qquad [4]$$

For incremental resistor deviations from matched conditions, the four resistor sensitivity factors have the same magnitude described by

$$S_x = \frac{1}{1+A}\left[\frac{V_{CM}}{V_X(FS)}\right] \qquad [5]$$

where

$$A = \frac{R_3}{R_1} = \frac{R_4}{R_2} \qquad [6]$$

Equations [4] and [5] can be used to establish the effect of a resistor error on the output voltage, V_o. In the present SSVC design, all four resistors are equal in magnitude and, by equation [6], A = 1.0. For a Ag-Zn cell, $V_X(FS)$ = 2.0 V, and V_{CM} for the SSVC is limited to 24 Vdc. Hence, S_x as given by equation [5] becomes

$$S_x = \frac{1}{1+1}\left(\frac{24}{2}\right)$$

$$S_x = 6 \qquad [7]$$

A value of sensitivity coefficient of 6.0 implies that a 1% change in any of the four feedback resistors R_1 through R_4 will produce a 6% change in the differential amplifier output voltage.

2.4 DESIGN CRITERIA

A review of the Ag-Zn cell charging characteristics, in particular the voltage spike problem, and the limitations and shortcomings of the existing SSVC design resulted in the establishment of the baseline SCP design criteria summarized in the following paragraphs.

2.4.1 Packaging

The SCP shall be of modular construction design to enhance direct attachment to the Ag-Zn cells used in Task II testing.

2.4.2 Functional Requirements

The primary design requirement for the SCP is to provide full cell level protection against overcharge and overdischarge by means of bypass circuits capable of switching and sustaining a 20-A current. While designed specifically for Ag-Zn secondary cells, the design shall be flexible enough to permit adaptation to other rechargeable cells. The SCP shall be capable of providing individual cell protection for battery voltages up to 38.7 Vdc (18 Ag-Zn cells in series). This protection shall be accomplished by terminating charge or discharge when the cell voltage reaches a preset limit.

1) Operating Modes - The SCP shall have two operating modes, latch and pulse.

   a) Latch Mode - When operating in the latch mode, the SCP shall be capable of automatically switching cells out of circuit only. The SCP shall switch cells into the circuit only after reception of an external command.

   b) Pulse Mode - When operating in the pulse mode, the SCP shall be capable of automatically switching cells in and out of the circuit. Cells shall be automatically switched into circuit following a time delay, which is initiated by the return of the cell voltage to an in-limit condition. The SCP shall be configured in the latch or pulse mode of operation by means of a switch mounted on the SCP.

2) Charge Protection - To prevent premature charge termination due to the monoxide-to-peroxide transition overvoltage, the SCP shall incorporate a time delay during which switching operation is inhibited. The operation of the SCP is illustrated in figure 15. When the cell voltage is below the enable threshold voltage, the charge limit detection function (but not the discharge limit detection function) is inhibited. When the cell voltage rises to the enable threshold voltage, a timer is started that establishes a time delay, T1. After the time delay T1, the charge limit detector is enabled and a subsequent increase in cell voltage to the charge voltage limit results in immediate switching of the cell to an open circuit condition.

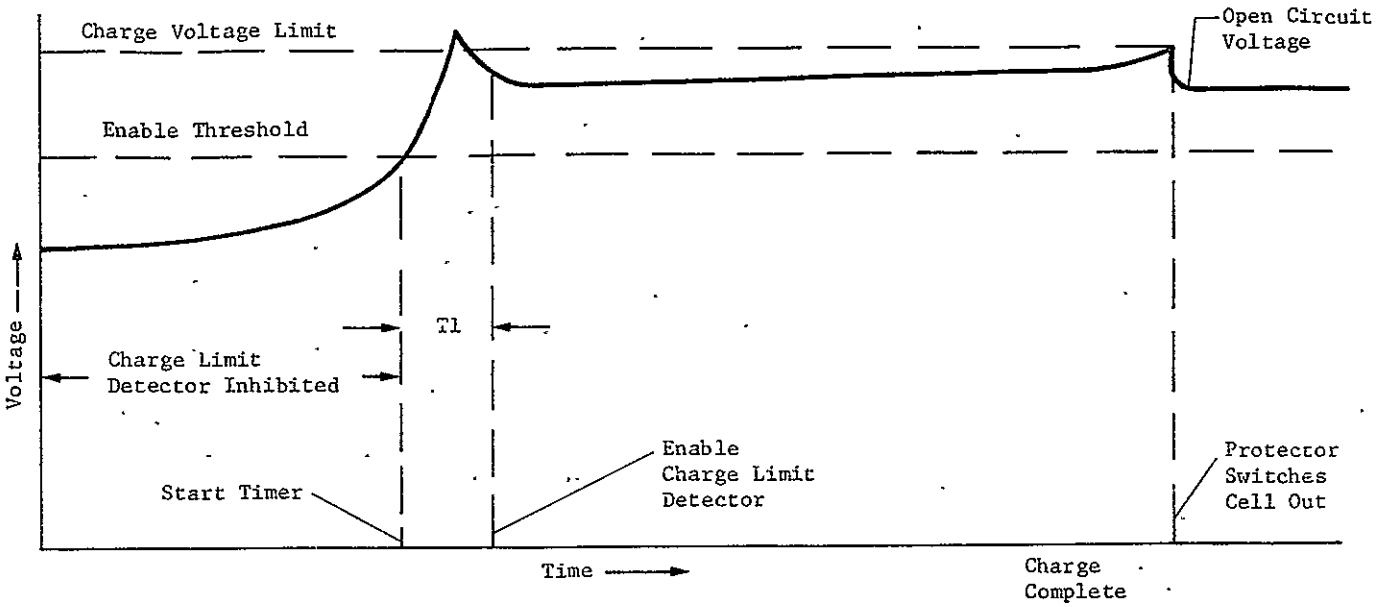


FIGURE 15 CELL PROTECTOR OPERATION DURING CHARGE

If the cell voltage remains above the enable threshold voltage after charge completion, and the cell is then returned to the charge mode by remote command, the SCP will immediately switch the cell to an open circuit condition, without the time delay T1, after the cell voltage reaches the charge voltage limit.

If the cell voltage falls below the enable threshold voltage after charge completion, and the cell is then returned to the charge mode by remote command, the SCP will switch the cell to an open circuit condition after a time delay, T1.

3) Discharge Protection - End of discharge is indicated by a decay in cell voltage to a discharge voltage limit. After the cell voltage falls to the discharge voltage limit, the SCP shall immediately switch the cell to an open circuit condition without delay.

4) Out of Limit Override - The ability to override the SCP protection function and operate the battery as a standard battery without protection shall be incorporated in the SCP design.

5) Power - The SCP shall be capable of operation from either a single floating power supply or from separate positive and negative supplies referenced to battery negative.

6) Battery Interrupt - During discharge, the SCP shall not interrupt current flow through a series-wired battery group of cells when switching a cell out of circuit. During charge, the SCP may momentarily interrupt battery current when switching a cell out of circuit.

7) Internal Protection - The SCP shall be designed for maximum protection against circuit damage due to inadvertent short circuits or misconnection at the SCP interface.

8) Operating Range - The SCP shall be capable of protecting an individual cell in an 18-cell series-wired Ag-Zn battery group.

9) Operating Temperature - The SCP shall be capable of operating in a temperature of 0 to 50° C.

10) Power Transients - The SCP shall not cause improper relay transfer when power is removed.

11) External Commands - The SCP shall respond to two external commands: one to switch a cell into circuit (CELL IN CMD) and one to switch a cell out of circuit (CELL OUT CMD).

12) Remote Cell Monitor - The SCP shall allocate two connector pins to be used by remote instrumentation for cell voltage monitoring. One connector pin shall be attached to the cell positive terminal [CELL MONITOR (+)]. The other pin shall be attached to the cell negative terminal [CELL MONITOR (-)].

13) Remote Status Monitoring - The SCP shall allocate two connector pins to provide means to indicate cell status (i.e., whether the cell is in circuit or out of circuit) to remote instrumentation. In-circuit status shall be indicated by energizing the MONITOR CELL IN pin and out-of-circuit status shall be indicated by energizing the MONITOR CELL OUT pin.

2.4.3 Performance Requirements

1) Voltage Sensing Requirements

   a) Charge Voltage Limit - The charge voltage limit shall be adjustable from 1.3 to 2.15 Vdc. Charge voltage limit detection shall be accurate to ±10 mV.

   b) Discharge Voltage Limit - The discharge voltage limit shall be adjustable from 0.5 to 1.35 Vdc. Discharge voltage limit detection shall be accurate to ±10 mV.

   c) Enable Threshold Voltage - The enable threshold voltage shall be 1.75 ±0.05 Vdc.

2) Enable Time Delay - The delay from the time an enable threshold voltage is sensed until the SCP charge limit detector is enabled shall be 12 to 20 min (16 min nominal).

3) Operating Voltage Range - The SCP shall perform charge and discharge voltage limit detection and cell switching in the

presence of common mode voltages up to 38.7 Vdc (2.15 Vdc average for 18 cells in a battery pack).

4) Operating Current Range - The SCP shall operate as specified for battery currents up to 20 A.

5) Power Dissipation - The SCP shall be designed for minimum power consumption but shall not require more than 0.42 W in the monitor condition and not more than 5.4 W during switching.

6) Pulse Mode Time Delay - When the SCP is in the pulse mode of operation, the delay from the time the cell voltage returns in limit from an out-of-limit condition until the SCP switches the cell into circuit shall be 3 to 5 min (4 min nominal).

7) External Commands - The SCP shall respond to a switch closure from CELL IN CMD or CELL OUT CMD to supply voltage negative.

8) Status Monitor - The SCP shall internally connect supply voltage positive [V_S (+)] to the CELL IN MONITOR or CELL OUT MONITOR connector pins as indicated in the schedule below.

Cell Status	Monitor Cell In	Monitor Cell Out
In-Circuit	V_S (+)	Open
Out-of-Circuit	Open	V_S (+)

2.4.4 Electrical Connectors

The SCP shall have two connectors: primary and secondary. The connector pin assignment shall be as shown in table 2.

TABLE 2 SCP CONNECTOR PIN ASSIGNMENT

Description	Primary J1-	Secondary J2-
V_S (+)	2	--
Battery positive	7	--
V_S (-)	3	3
Cell in command	4	4
Cell out command	8	8
Cell monitor (-)	5	5
Cell monitor (+)	9	9
Cell out monitor	1	1
Cell in monitor	6	6

2.5 SCP DESIGN

Figure 16 is a functional block diagram of the SCP. A single SCP is attached to an individual cell, and a magnetic latching relay is used to switch the cell into or out of a series-wired battery configuration. Cell voltage is monitored for in-limit or out-of-limit conditions by the cell monitor. An out-of-limit indication signal (OLI in figure 16) is sent to the relay control whenever cell conditions warrant, causing the cell to be switched out of circuit. The comparators are connected directly to the cell via the voltage monitor leads attached to the cell terminals. In this way, errors due to voltage drop in the relay and cell interconnection circuitry are eliminated. Cell voltage monitoring points are also connected to these potential leads for use by remote instrumentation. The external command to switch a cell out of circuit (CELL OUT CMD) is connected to the cell monitor. The presence of a CELL OUT CMD causes the cell monitor to generate an OLI signal to initiate that the SCP is switching the cell out of circuit.

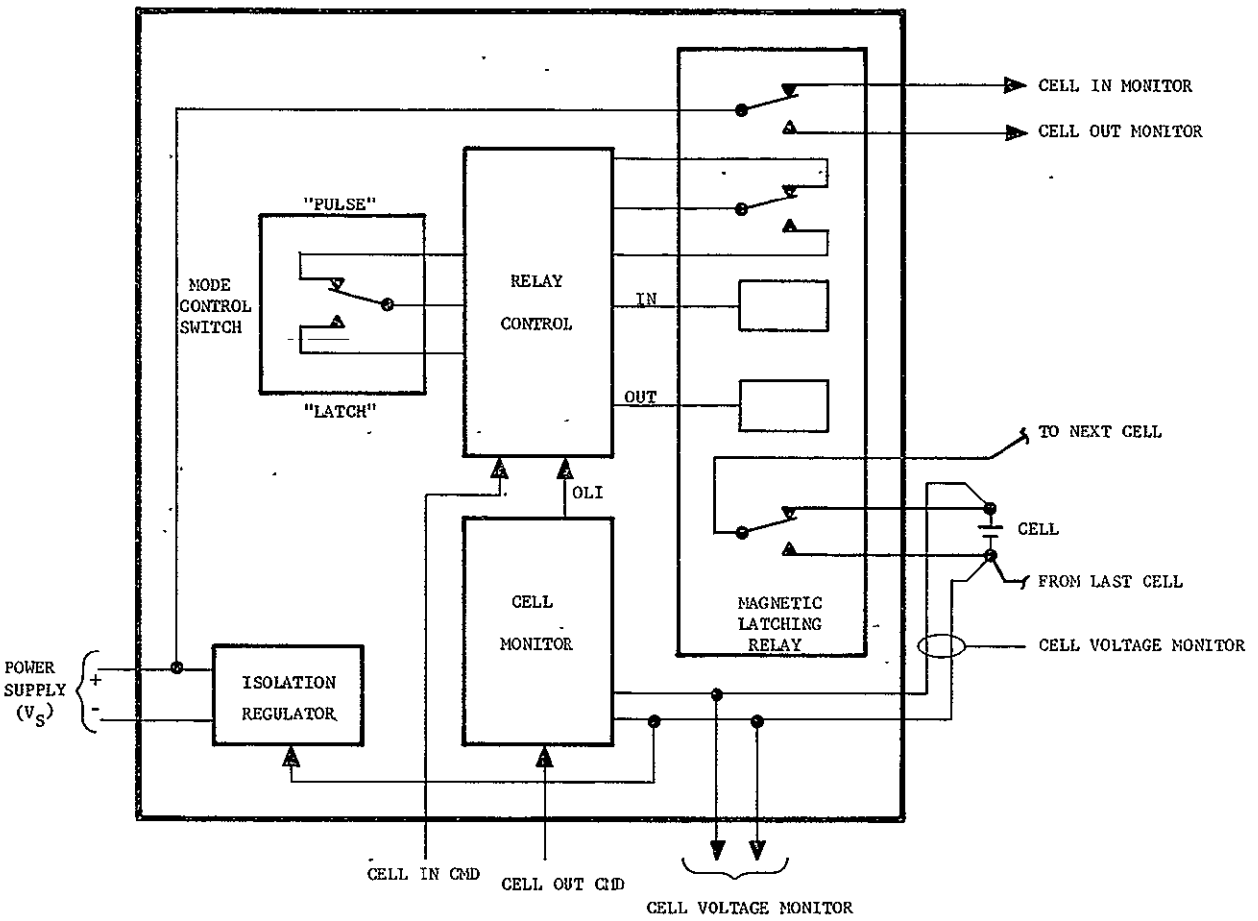


FIGURE 16 SIMPLIFIED SCP BLOCK DIAGRAM

The relay control generates relay commands to switch the cell in or out of circuit. The mode switch connected to the relay control determines the operating characteristics of the SCP for a cell that is out of circuit. If the mode switch is in the LATCH position, a cell out of circuit will remain so until returned to circuit by an external command (CELL IN CMD). If the mode switch is in the PULSE position, a cell switched out of circuit will automatically be returned to circuit after a 4-min delay.

One set of relay contacts is used by the relay control to sense cell status (in or out of circuit). A third set of contacts is used to provide an indication of cell status to remote instrumentation.

An isolation regulator is used to provide floating bias voltages (referenced to the cell negative terminal) to power cell monitor and relay control circuitry. Two bias voltages, VB (+) and VB (-) are generated from a single power supply source, V_S.

2.5.1 Design Approach - Figure 17 is a diagram of the SCP that shows the essential features of the key blocks in figure 16. As shown in figure 17 cell terminals are brought to the cell monitor via potential leads. Diode CRA connected across these leads prevents bus dropout during discharge when the relay switches the cell out of circuit.

The cell monitor circuit compares the cell voltage to preset limits and generates an out-of-limit indication (OLI in figure 16) based on these limits.

The common mode range and accuracy problems associated with the SSVC design have been avoided in the SCP by incorporation of an isolation voltage regulator that establishes a variable reference (signal ground) for the detection circuitry that is equal to the cell negative terminal potential. The full cell voltage thus appears at the inputs of three voltage comparators without attenuation or conditioning by a differential amplifier.

The comparators detect three cell voltage levels critical to protector operation:

$\overline{\text{OLL}}$ - a true-low signal indicating that the cell voltage is out-of-limits low, that is, below the discharge cutoff limit;

OLH - a true-high signal indicating that the cell voltage is out-of-limits high, that is, above the charge cutoff limit;

$\overline{\text{PER}}$ - a true-low signal indicating that the cell voltage has risen above the enable threshold voltage and is entering

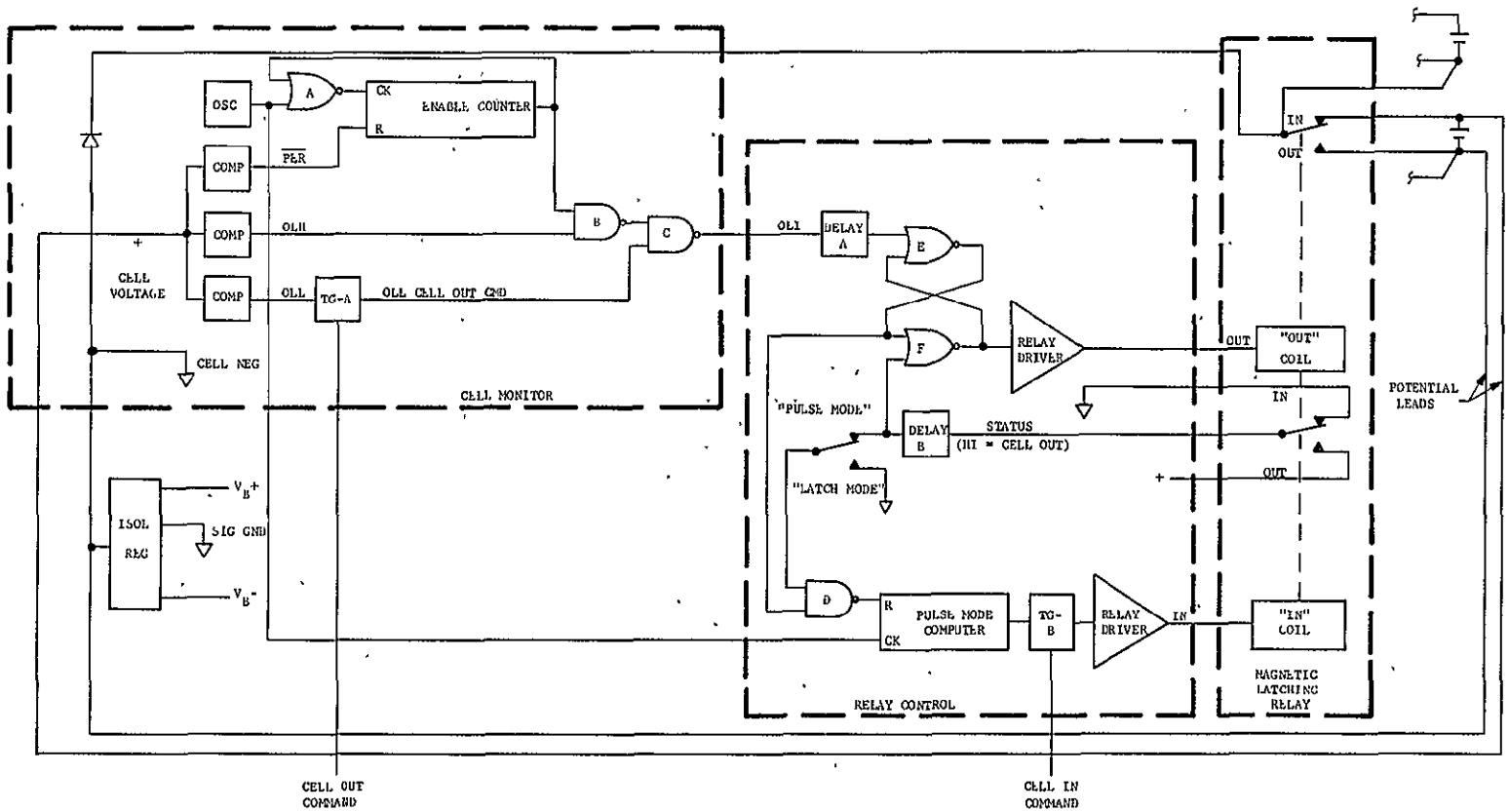


FIGURE 17 SINGLE-CELL PROTECTOR BLOCK DIAGRAM

the peroxide regions of operation shown in figure 2.2-10. The appearange of $\overline{PER}$ means that the cell is encountering the voltage spike and may operate a premature OLH signal.

The appearance of the $\overline{PER}$ signal allows the enable counter to time out and generate the ENABLE signal. The time delay from the appearance of $\overline{PER}$ until ENABLE is generated is the time delay T1 in figure 2.4-1.

The ENABLE, OLH, and $\overline{OLL}$ signals are combined in gates B and C to generate the out-of-limit indication signal (OLI). OLI is produced whenever an out-of-limit high and an ENABLE signal are present, or when an external CELL OUT command is given. That is

$$OLI = \overline{OLL} + OLH\ ENABLE + \overline{CELL\ OUT\ CMD} \qquad [9]$$

Equation 9 can be reduced by an elementary transformation to

$$OLI = (OLL)(CELL\ OUT\ CMD)\ \overline{(OLH\ ENABLE)} \qquad [10]$$

Equation 10 is the actual logic equation implemented in figure 17 with NAND gates B and C and transmission gate TG-A.

The OLI signal causes the relay "OUT" coil to be pulsed via the cross-coupled latch consisting of gates E and F--and thus switches the cell out of circuit. If switch S1 is in the LATCH position, the cell will remain out until returned to circuit by an external command (CELL IN CMD). If S1 is in the PULSE position, switching the cell out of circuit will cause the pulse mode counter to begin counting. When the pulse mode counter times out, the relay "IN" coil will be pulsed and the cell automatically returns to circuit.

2.5.2 Voltage Comparators - Figure 18 is a detailed schematic of the voltage comparator circuitry. A precision 2.42-V reference voltage is generated by the voltage regulator consisting of U2-A and associated circuitry. VR2 is a 6.4-V temperature-compensated reference diode that ensures a very stable voltage at the output of U2-A. The VR2 bias current is primarily determined by R4 and is itself regulated because it is obtained from the regulator output voltage. Resistor R35 provides a trickle current that ensures that the regulator starts at power up. Resistors R5, R6, R7, and R8 compose a multiple output voltage divider that provides the stable bias voltages required for high performance circuit operation. R6 is selected in test to trim the 2.42-V output of U1-D. The 1.75-V output at the junction of R7 and R8 sets the IN H trip level. Buffer amplifier U1-A establishes an ANALOG REF voltage equal to the potential of the cell negative terminal.

The three comparators are U2-B, U2-C, and U2-D. Comparator U2-B generates the INH signal and switches low whenever the cell voltage

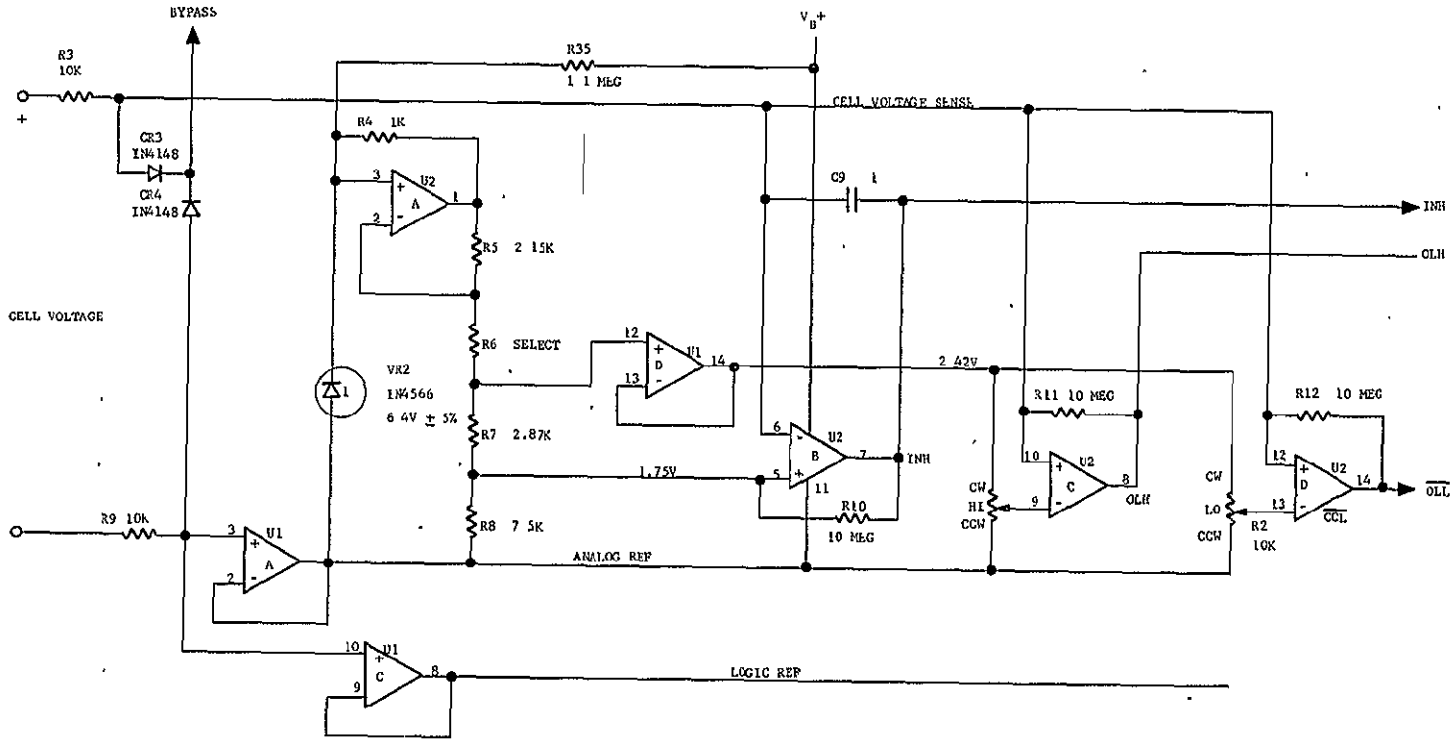


FIGURE 18 COMPARATOR CIRCUITRY

exceeds the 1.75-V reference level. The IN H switching level is not adjustable. Comparators U2-C and U2-D generate the OLH and OLL signals. The OLH and OLL switching levels can be varied between 0 and 2.42 V by adjusting potentiometers R1 and R2. A resolution of adjustment to approximately 1.0 mV can be obtained. All three comparators have a small (<10 mV) hysteresis (provided by R10, R11, and R12) to guarantee snap action at switching.

A LOGIC REF voltage equal to, but isolated from, the ANALOG REF voltage is generated by U1-C for use by the digital circuitry. By providing two isolated reference voltages in this manner, switching noise present on LOGIC REF cannot couple onto ANALOG REF and cause erroneous switching in the comparators.

Diodes CR3 and CR4 provide circuit protection in case the SCPs are attached to battery cells with power removed. Under these conditions, current flowing through R3 and R4 is shunted away from the operational amplifier inputs through the BYPASS circuit.

2.5.3 Oscillator - The clock signal for the ENABLE and pulse mode counters is generated by the square-wave oscillator circuit shown in figure 19.

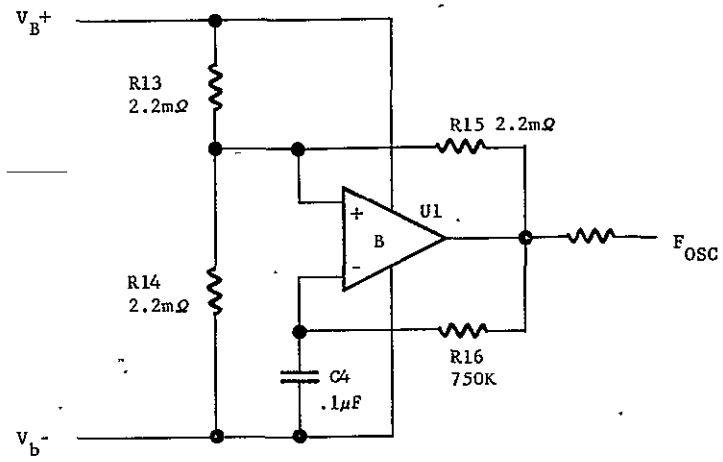


FIGURE 19 OSCILLATOR CIRCUIT

2.5.4 Relay Control Circuit - The relay control circuit operates on the OLI signal from the cell monitor circuit, generates the appropriate time delays required for circuit operation, and issues pulses to the relay coils that command switching. The relay control circuit in figure 17 is shown schematically in figure 20.

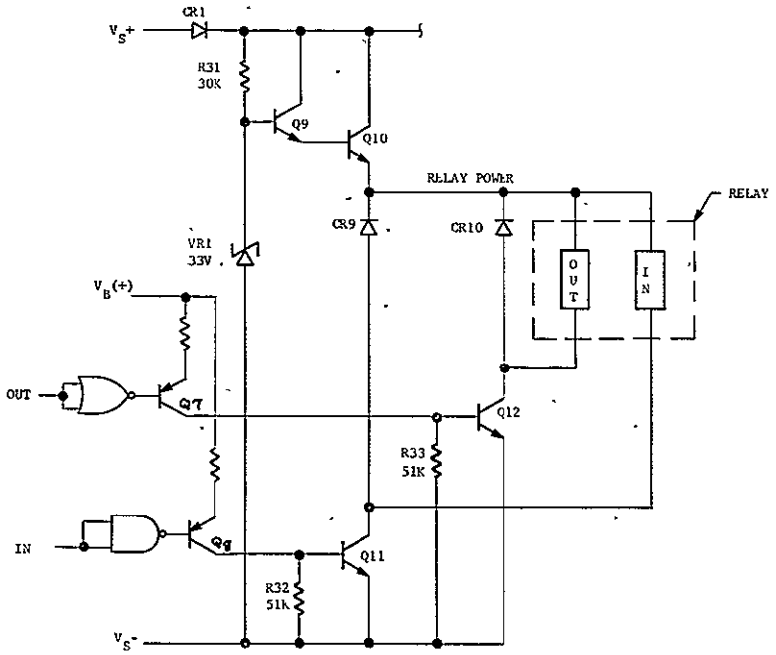


FIGURE 20 RELAY DRIVER

The deciding factor in the selection of magnetic-latching relays for the SCP was their zero standby power consumption. However, this advantage is counterbalanced by the special operational requirements associated with their use that do not pertain to nonlatching relays. Foremost among these requirements is the need to know the position of the relay (cell in or out of circuit) because, with no power applied to either the IN or OUT coil, the relay can be in either position, this position cannot be conclusively ascertained from available circuit signals in the relay control circuit. The possibility of confusing the relay control logic circuitry and damaging the SCP and/or cell is thus raised. For this reason, a spare set of relay contacts was used to provide positive information on the relay state (the STATUS signal in figure 17.

Another requirement peculiar to the use of the magnetic latching relay is that the coil voltage must be pulsed and not continuously held. A continuous voltage applied to a coil will not damage the latching relay, but would negate the advantage of low power consumption offered by its use and would of course violate the SCP power consumption design requirement. Furthermore, during SCP development, advantage was taken of minimizing the circuitry involved in pulsing the relay coils. Consequently, in the SCP design, a continuous voltage applied to a relay coil can cause the relay driver to fail due to excessive power dissipation.

Resolving the concerns with assuring knowledge of relay position and coil pulsing under all hypothetical circuit conditions resulted in a relay control circuit of somewhat greater complexity than that required for a nonlatching relay. The SCP relay control circuit shown in figure 20 assures that:

1) When an OLI signal is received and a relay OUT command issued, the relay coil will receive a pulse wide enough to assume relay switching--relay switching will occur in spite of the loss of the OLI signal before completion of the relay switching action;

2) Once the relay has switched states (either OUT or IN), relay coil power will always be removed (i.e., relay coil power cannot be continuously held).

Operation of the relay control circuit is best illustrated by considering the logic equations for the coil OUT and IN signals. In terms of the signals defined in figure 17, the coil OUT signal equation is

$$OUT = \overline{STATUS} \bullet (OLI + OUT) \qquad [11]$$

The OUT signal present on both sides of equation 11 assures latching operation. That is, once the OUT signal is initiated by the OLI signal, it will remain--even if OLI is removed--until the loss of the STATUS signal occurs, indicating that the relay bus switched and the cell is out. Once the relay bus transfers and the STATUS signal switches low, the OUT signal is automatically removed. If an OLI signal were received when the STATUS signal was low (indicating that the cell was out of circuit), the OUT signal would not be given and the relay coil would not be pulsed. Useless pulsing of the relay coils is thus avoided.

The Delay A block in figure 17 prevents OLI errors (due perhaps to switching of other cells in the battery string) from causing a cell to be switched out of circuit. The Delay B block ensures that the OUT pulse to the relay coil is not removed during the relay contact transition time. Both Delay A and Delay B are realized with simple RC networks.

The equation for the relay IN signal in figure 17 is

$$IN = \text{PULSE MODE} \bullet \overline{OLI} \bullet OUT \bullet \text{PULSE MODE DELAY} + \overline{\text{CELL IN CMD}} \qquad [12]$$

A word statement of equation 12 is that an IN coil signal can be issued if a $\overline{\text{CELL IN CMD}}$ signal (true low) is given or if the SCP is configured in the PULSE mode of operation, the pulse mode time delay is satisfied, an OLI is not present, and an OUT signal is not being issued.

In figure 20, Q9, Q10, R31, and VR1 constitute a coarse voltage limiter that prevents the relay coil voltage from exceeding

approximately 32 V. The relay coils are driven by Q11 and Q12 that in turn are driven by Q7 and Q8. Q7 and Q8 provide the required level translation of the IN and OUT signals from the floating SCP monitor and control circuitry to the Q11 and Q12 drive circuitry.

2.5.5 Isolation Voltage Regulator - The isolation voltage regulator provides positive and negative floating bias voltages for the detector and control circuitry. These bias voltages are referenced to the negative terminal of the cell being protected by the SCP. Figure 21 is a schematic diagram of the regulator. A single power supply, V_S, is required to power the SCP.

Blocking diode CR1 is used to provide protection against SCP damage due to inadvertent reversal of the V_S power leads. The R18, R19 resistor divider is used to balance the V_S source with respect to the battery. For proper circuit biasing, the junction of R18 and R19 is connected to the battery negative terminal to correctly fix all circuit bias voltages with respect to the battery.

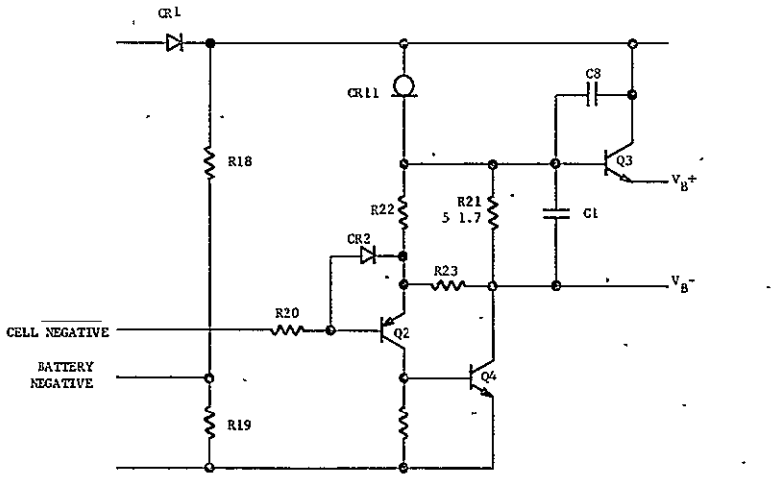


FIGURE 21 ISOLATION VOLTAGE REGULATOR

Transistors Q2, Q3, and Q4, with their associated circuitry, constitute the regulator. The nature of the feedback is such as to control the Q2 base voltage equal to the voltage of the negative terminal of the cell being protected (CELL NEGATIVE in figure 21). The two bias voltages, V_B+ and V_B−, are then generated with reference to CELL NEGATIVE. CR11 is a constant-current diode, and most of its current flows through the R21, R22, and R23 network to establish fixed bias voltages. R21 was selected in test to adjust V_B+ and V_B− to the required levels.

R20 and CR2 were added to protect the SCP from damage if power is removed when an SCP is connected to a battery.

2.6 PACKAGING DESIGN AND FABRICATION

2.6.1 Mecahnical Design Considerations - Basic SCP packaging criteria are summarized as follows.

1) Construction of the SCP shall be sufficiently rugged to withstand the normal handling expected in a laboratory environment.

2) All internally mounted components shall be readily accessible to facilitate circuit repairs or part replacement.

3) The circuit shall perform its function reliably over its expected lift with minimum failure rate and downtime.

4) The SCP must be configured to provide minimum voltage drop between the SCP and the battery cell.

5) Fabrication cost and size of the SCP shall be kept to a minimum, consistent with the above requirements.

2.6.2 Packaging Design Description - Of the many packaging concepts evaluated during the preliminary design phase, only the modular approach offered the flexibility necessary to meet the basic requirement of protecting one or more cells. The modular design also permits much broader use because the cells may be located and tested in remote test areas.

The requirement for the SCP to be placed close to the cell was the most significant factor in determining SCP configuration. The width of the SCP was constrained by the width of the cell to be tested, and the height was determined by the wire routing to the cell terminals. To reduce the voltage drop from the cell to the SCP, wire lengths were kept to a minimum and AWG 12 wire was used.

Two redundant subminiature connectors provide interface to the power supply and the control and display panel. A two-position switch on the top of the case is provided for pulse or latch mode of operation. The two electrical connectors, J1 and J2, are placed so that when the SCPs are in a test configuration they can be freely mated and unmated. The trim pots, accessible from the bottom of the SCP, provide manual adjustment for the upper and lower voltage limits. The SCP uses three double-sided PC boards (figure 22) mounted on threaded standoffs. The partitioning of circuits with respect to their functions both within themselves and in relation to adjacent circuitry was considered and incorporated in the package design. Gold-plated fingers are provided on the ends of the PC boards to facilitate board-level functional testing. Each board is also keyed to preclude the possibility of mismating in the test fixture. Board design is in compliance with the part mounting

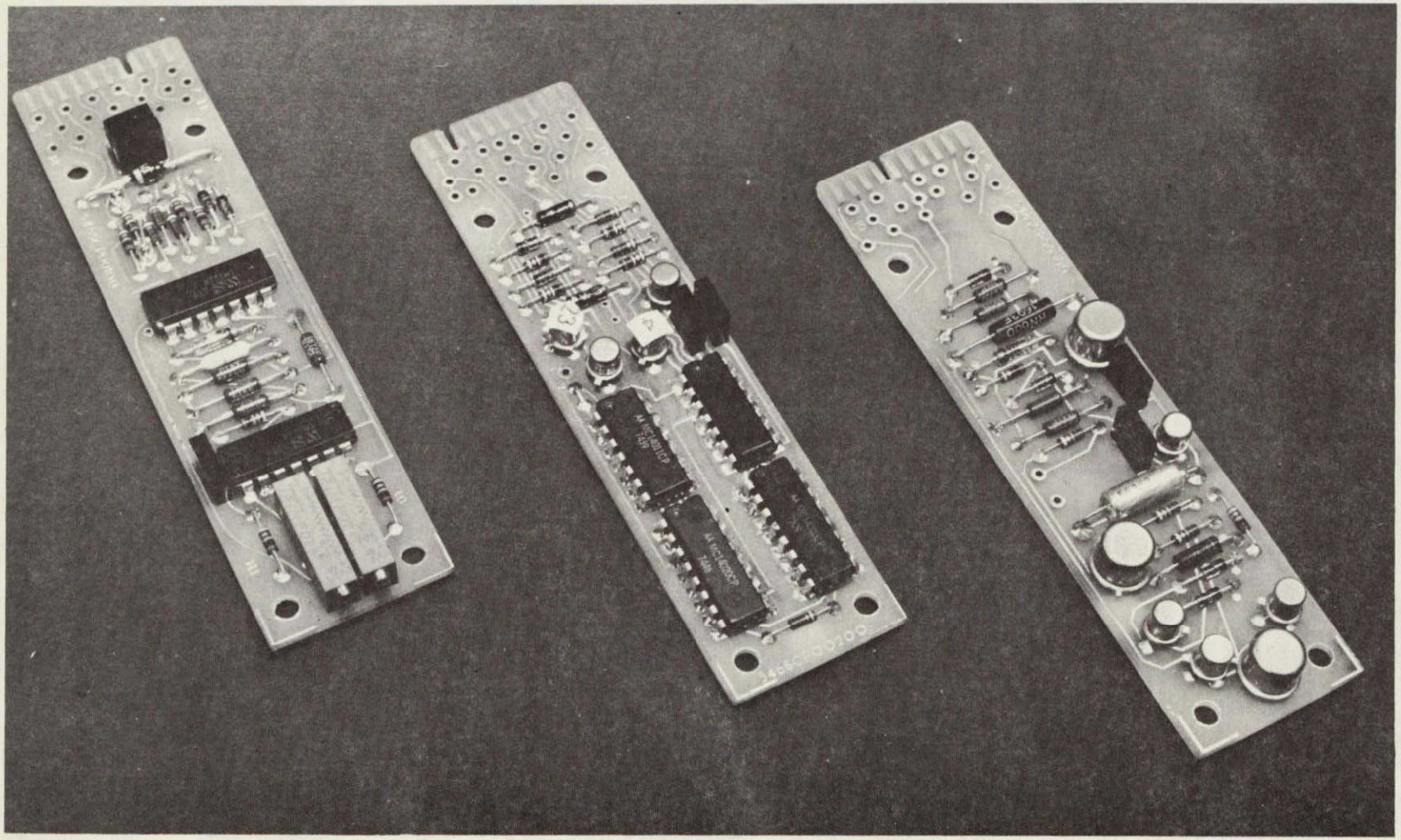


FIGURE 22 THREE DOUBLE-SIDED PC BOARDS USED IN SCP

and interconnection requirements of NHB 5300.4 and the PC board design specification, MSFC STD-154A. Plated-through holes used only for interfacing connections are not filled, and Z-bars are not used. The rationale for this decision is based on extensive testing and analysis by Martin Marietta that has shown unquestionably that an unsupported plated-through hole provides a thoroughly reliable interfacial connection.

The case is welded sheet metal. Aluminum was selected because of its excellent welding and forming characteristics. It also provided the necessary thermal conductance. For aesthetic reasons, the case exterior was painted the same color as the battery cells.

Board interconnections are made using AWG 26 stranded insulated wire terminated in plated-through holes and at solder terminals on the relay and switch. The two prewired encapsulated connectors are ITT Cannon MDB1-95H001 connectors. The assembly is wired with adequate service loops to allow the PC boards to be withdrawn from the box and fanned out for access to all electronics for trouble shooting and functional test.

2.6.3 Fabrication - Figure 23 shows the assembly sequence for fabricating the SCP, starting with PC board assembly. The electrical components are mounted on the PC boards and soldered in place to the requirements of the Martin Marietta Assembly Process STP85132. The assembler uses temperature-controlled soldering irons to reduce the possibility of damaging or degrading the reliability of heat-sensitive components during soldering. The boards are then inspected and functionally tested.

After completion of board-level tests, the PC boards, relay, switch, and connectors are placed in an assembly fixture for prewiring the assembly. Wires to the battery cell terminals are also soldered to the relay at this time. When soldering operations are complete, a detailed inspection and continuity tests are performed. The electronics are then installed in the case.

The first operation in the electronics installation is mounting the relay. It is banded to the case using a standard pneumatic transformer banding tool set to a banding tension of 207kPa(30 psig). The band not only furnishes an intimate thermal contact between the relay and case but also provides an inexpensive low-profile repairable mechanical support for the relay.

With the relay securely mounted to the case, the remainder of the electronics is installed and secured in place. A fit check is then performed to verify that the unit has not been degraded by pinched or damaged wires, wires bearing on sharp points, contamination, etc. Minimum clearance between components on the PC boards and protrusions on adjacent boards has been assured by control dimensions for PC board

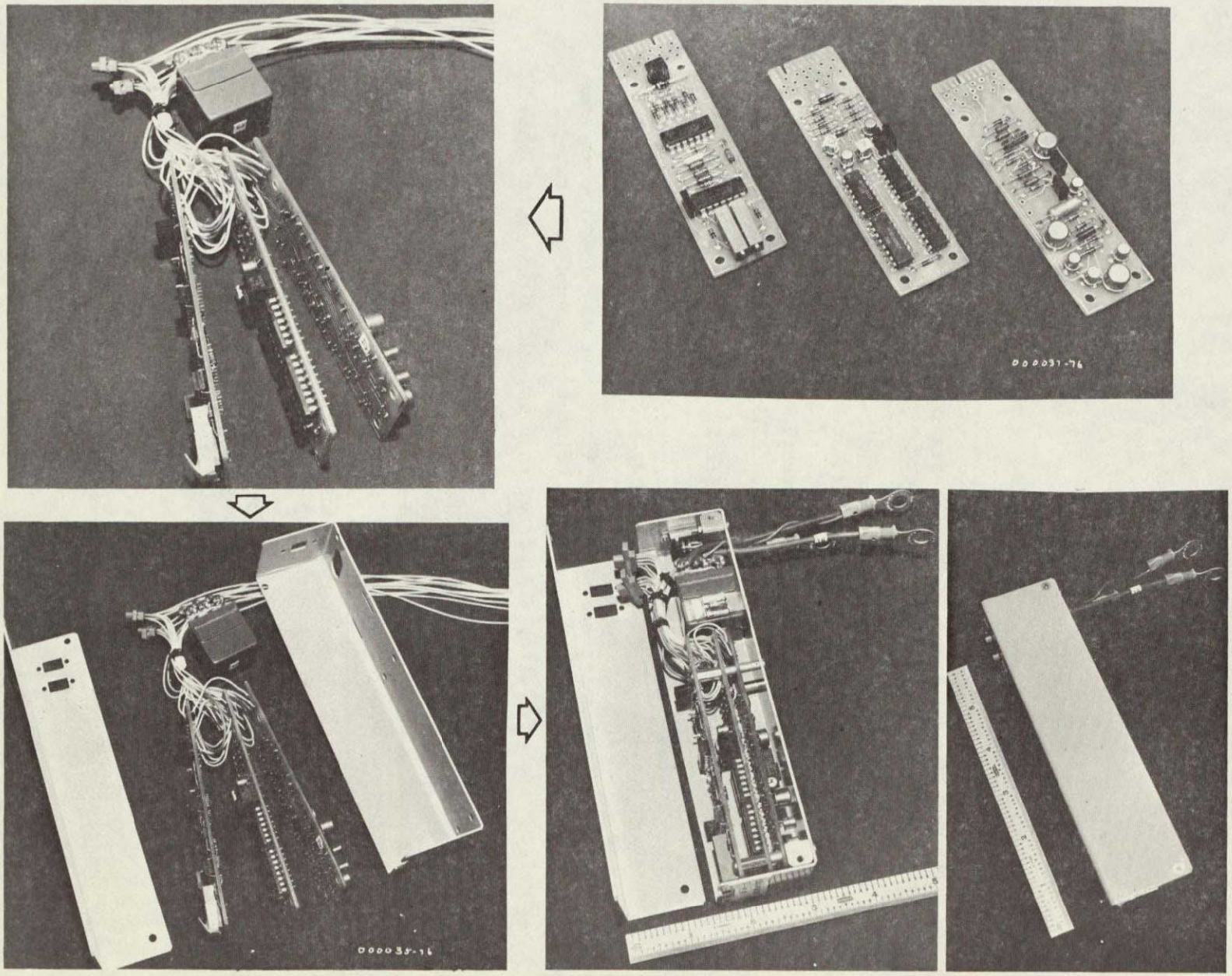


FIGURE 23. SCP FABRICATION, ASSEMBLY, AND TEST

assembly. The connectors are then installed on the cover, and the cover is mounted to the case.

2.6.4 Thermal Analysis - Thermal analysis of the SCP package was based on the following worst-case power dissipation levels:

Electronics - 0.8 W

Mag-latch relay contacts- 1.2 W at 20 A

Total - 2.0 W

Analysis of the SCP module in a worst-case 50°C free-air ambient environment showed transistor Q4 (in figure 21) to have the maximum junction temperature (123°C). The next highest temperature was 117°C at transistor Q3 junction. Both parts operate within the derated allowable temperature of 125°C. All other PC-board-mounted parts dissipate considerably less power, and therefore operate at much lower temperatures. The magnetic latching relay dissipates 1.2 W continuously under the worst-case condition of 20-A current. To provide good passive temperature control, the relay was banded to the case.

2.7 SCP DEVELOPMENT UNIT TEST RESULTS

One SCP development unit was fabricated and subjected to extensive evaluation testing. Some of the key data obtained from this test program are shown in figures 24, 25, and 26. Figure 24 shows comprehensive data on the charge and discharge limit accuracy over the extremes of common mode voltage V_{CM}, supply voltage V_S, and temperature. As evident from the data, SCP performance is well within established design limits.

The SCP development unit oscillator period stability over temperature is shown in figure 25. Because both the enable time delay and pulse mode time delay are integrally related to the oscillator period by digital countdown circuits, oscillator stability provides a direct measure of both delays. As can be seen from figure 25, the oscillator period varies only slightly with temperature. The sensitivity of the oscillator period to power supply voltage is negligible.

The SCP development unit standby current drain is shown in figure 26 as a function of supply voltage and temperature. The power supply current varies linearly with voltage and negligibly with temperature.

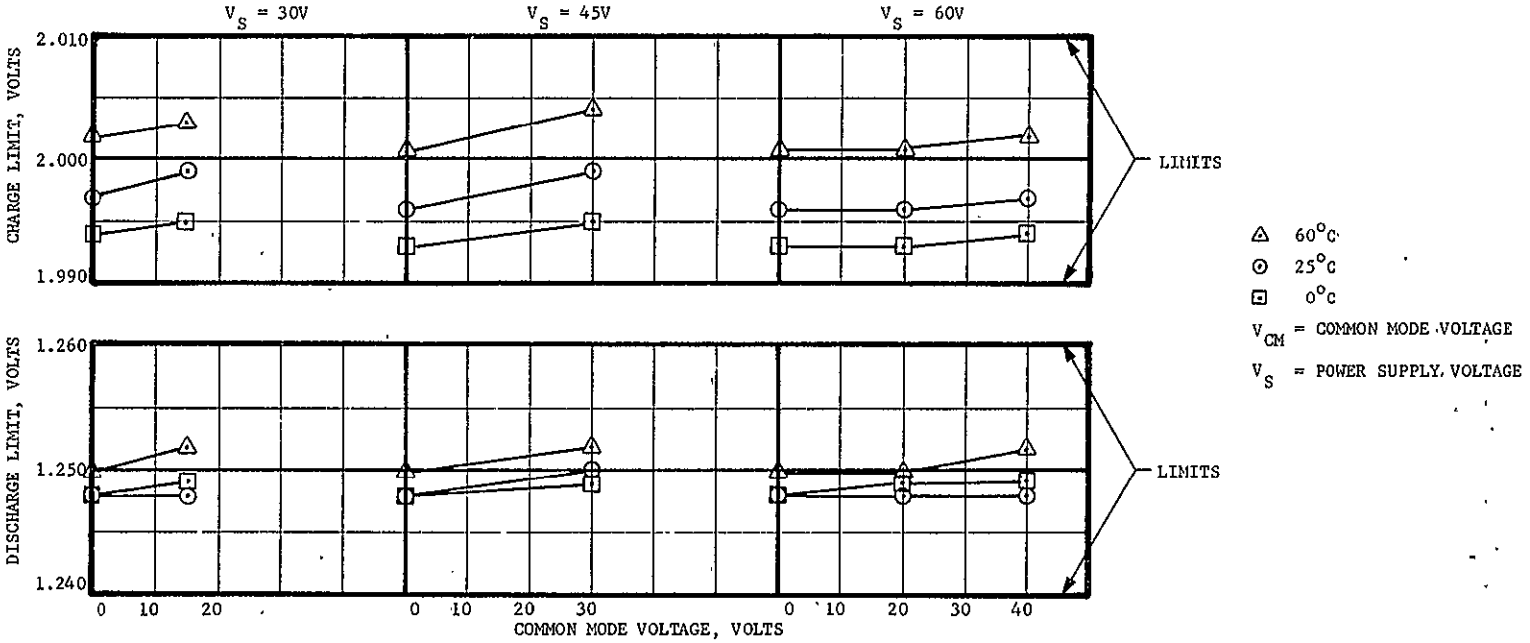


FIGURE 24 LIMIT-POINT ACCURACY OF SCP DEVELOPMENT UNIT

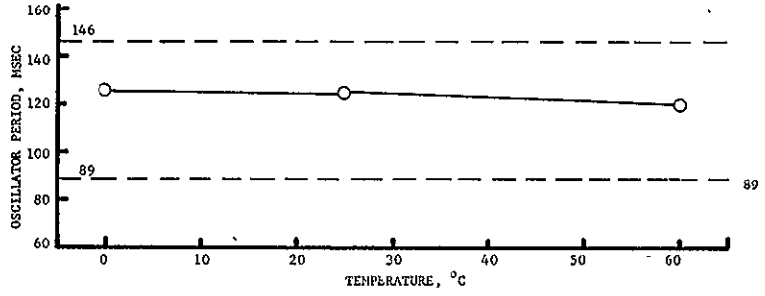


FIGURE 25 SCP DEVELOPMENT UNIT OSCILLATOR STABILITY

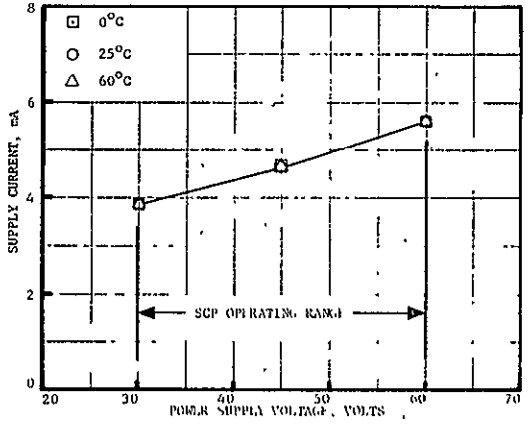


FIGURE 26 SCP DEVELOPMENT UNIT POWER SUPPLY CURRENT

2.8 SCP PRODUCTION UNIT TEST RESULTS

Figures 27 and 28 show acceptance test data for charge and discharge limit accuracy. Charge and discharge limits are initially calibrated with zero common mode voltage and with the power supply voltage 30 V. The charge limit is initially adjusted to 2.000 ±0.001 V and the discharge limit to 1.250 ±0.001 V. Charge and discharge limits are then measured over the extremes of common mode and supply voltage conditions listed in table 3. The data plotted in figures 27 and 28 are the maximum and minimum measurements obtained from the data shown in the test schedule. As seen from the figures, the spread in the data is typically 1.0 mV or less.

TABLE 3 RANGE OF COMMON MODE AND SUPPLY VOLTAGES

Limit checked	Supply voltage, V	Common mode voltage, V
Charge limit	30	0
	45	15
	60	0
	60	20
	60	40
Discharge limit	30	0
	45	15
	60	40

Figure 29 shows the pulse mode time delay for the production units. Enable delay time is not plotted but is related to the pulse mode delay by a factor of four due to the nature of the design. These delay times are not calibrated, and the spread in the data corresponds to unit-to-unit variations in the SCP oscillator period.

Figure 30 shows the SCP supply current for the standby mode of operation. Figure 31 shows the supply current during relay switching.

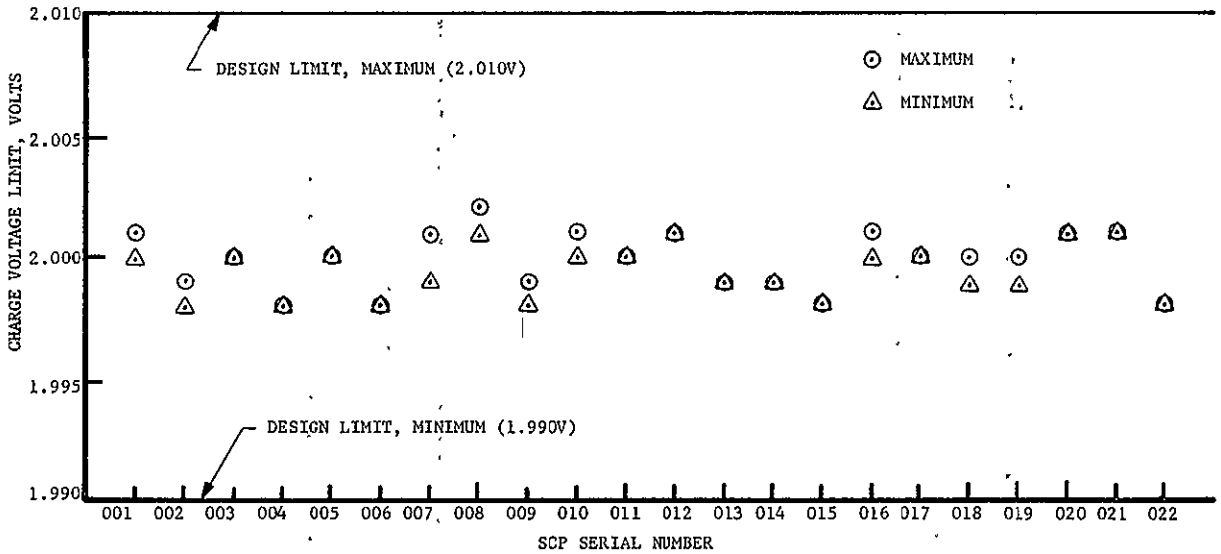


FIGURE 27 SCP CHARGE VOLTAGE LIMIT ACCURACY

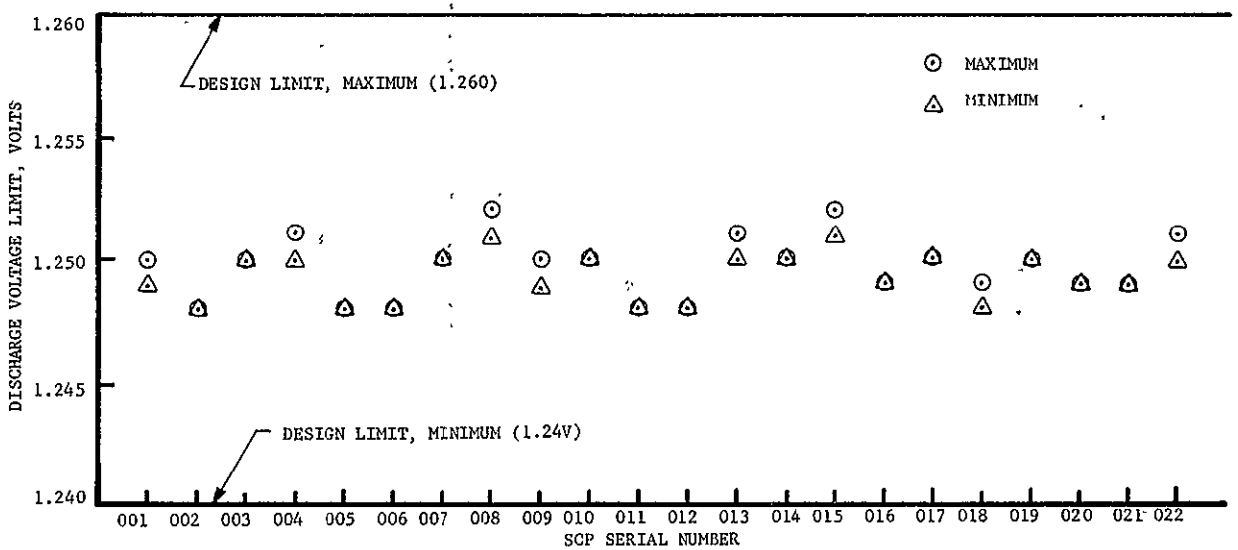


FIGURE 28 SCP DISCHARGE VOLTAGE LIMIT ACCURACY

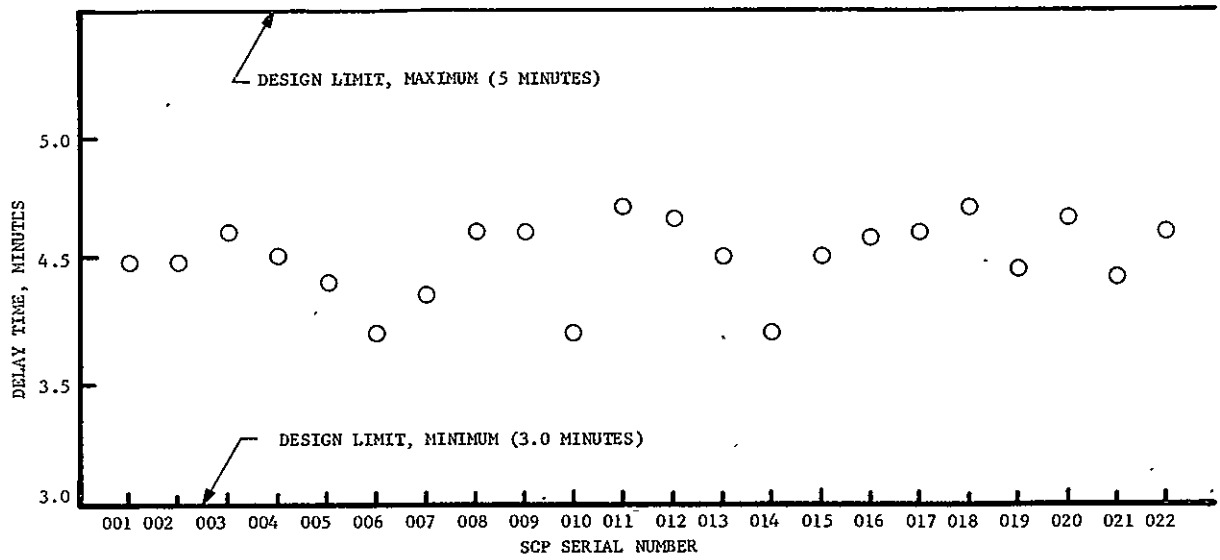


FIGURE 29 SCP PULSE MODE DELAY

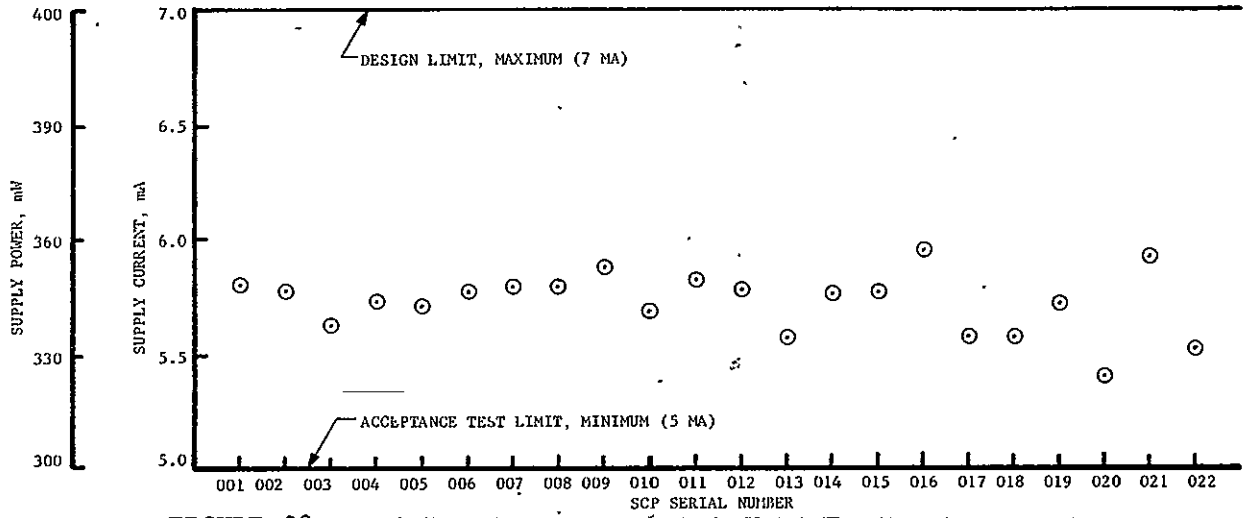


FIGURE 30 SCP STANDBY MODE SUPPLY POWER AND CURRENT AT 60-VDC SUPPLY VOLTAGE

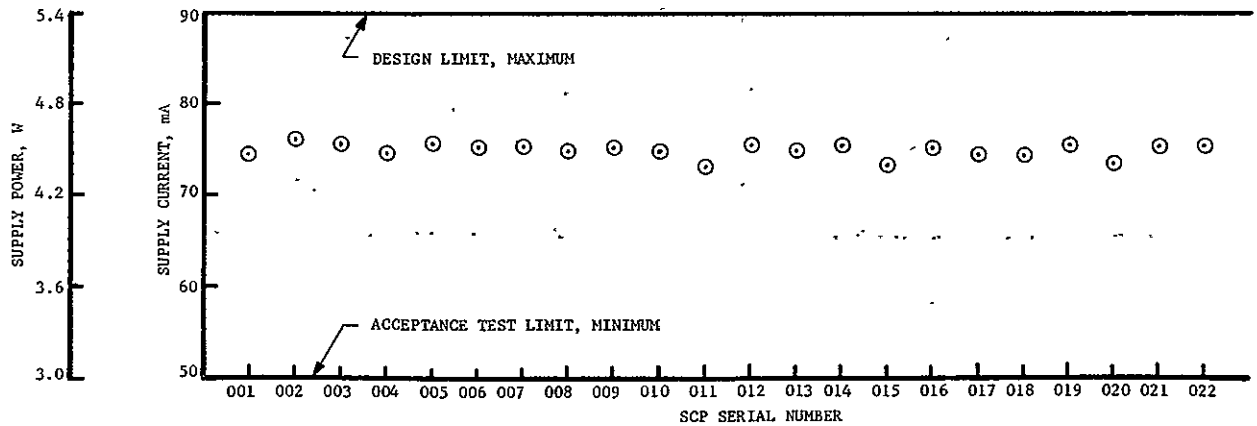


FIGURE 31 SCP SUPPLY POWER AND CURRENT DURING RELAY SWITCHING AT 60-VDC SUPPLY VOLTAGE

3.0 TASK II - BATTERY LIFE TESTING

3.1 TASK OBJECTIVE

The basic objectives of Task II were to assemble two battery packs to: (1) determine the effects of battery level and cell level control on extending the life of the 40-Ah silver-zinc batteries; 2) evaluate the performance of the SCPs by cycle testing on SCP-protected 18-cell battery packs. The scope of the task was defined by NASA LeRC as follows: "The single cell protector developed in Task I shall be applied to provide full single cell protection on a 28 volt battery made up of 40 ampere-hour silver-zinc cells. These cells shall be government furnished equipment (GFE) by NASA.

"Life cycle tests shall be made to compare the cell-protected battery against a standard, identical size battery that does not have single cell protection. Cells for the standard battery shall also be furnished by NASA as GFE. The cycle regime for this test shall be that of a synchronous-type orbit. Test shall consist of a 40% DOD, 1 cycle per day. Discharge at 13.3 amps for 1.2 hours followed by charging at 0.75 ampere for 22.8 hours. Cells shall be tested to failure or until the end of the contract period of performance. Failure is defined as the inability of the battery to perform the cuty cycle outlined above or whenever the average cell voltage of the battery falls below 1.25 volts/cell before the end of the 1.2 hour discharge period."

3.2 TEST CONFIGURATION

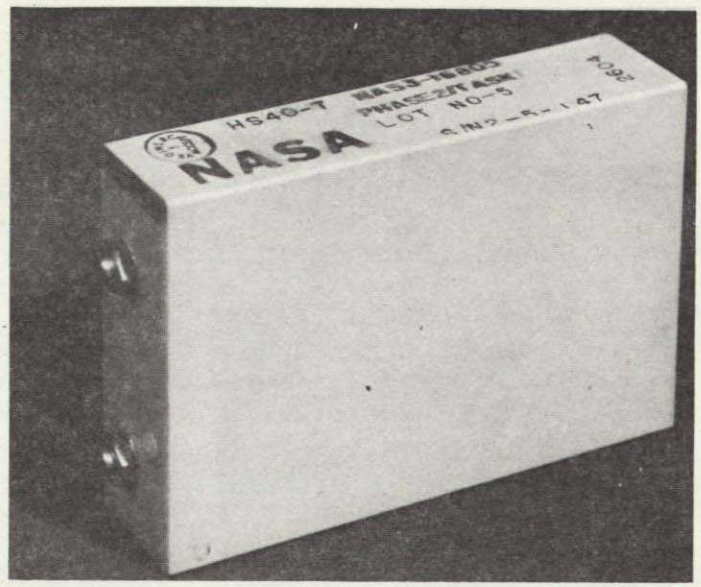
3.2.1 Battery Cell Description - The 40 Àh HS40-7 silver-zinc cells were manufactured by Yardney Electric Corporation for NASA Lewis Research Center. Fifty cells were provided to Martin Marietta as government furnished parts to support Task II testing. Figure 32 is a photograph of the cell showing its dimensions. Table 4 summarizes key design and physical features.

TABLE 4 KEY FEATURES OF HS40-7 SILVER-ZINC CELL

Capacity:	40 ampere hours
Number of plates:	6 positive - 5 negative
Separator Material:	Inorganic, fuel-cell grade asbestos
Header sealing:	Ultrasonically welded to provide complete seal

3.2.2 Group I Battery/SCP Configuration - The 18-cell battery pack designated Group I consists of two 9-cell assemblies. Each assembly is restrained between two steel plates. The cells are individually controlled and protected by the SCPs. Figure 33 shows the typical electrical connection of one SCP and one silver-zinc cell.

The control and display panel (C&D) in figure 34 provides the following functions:



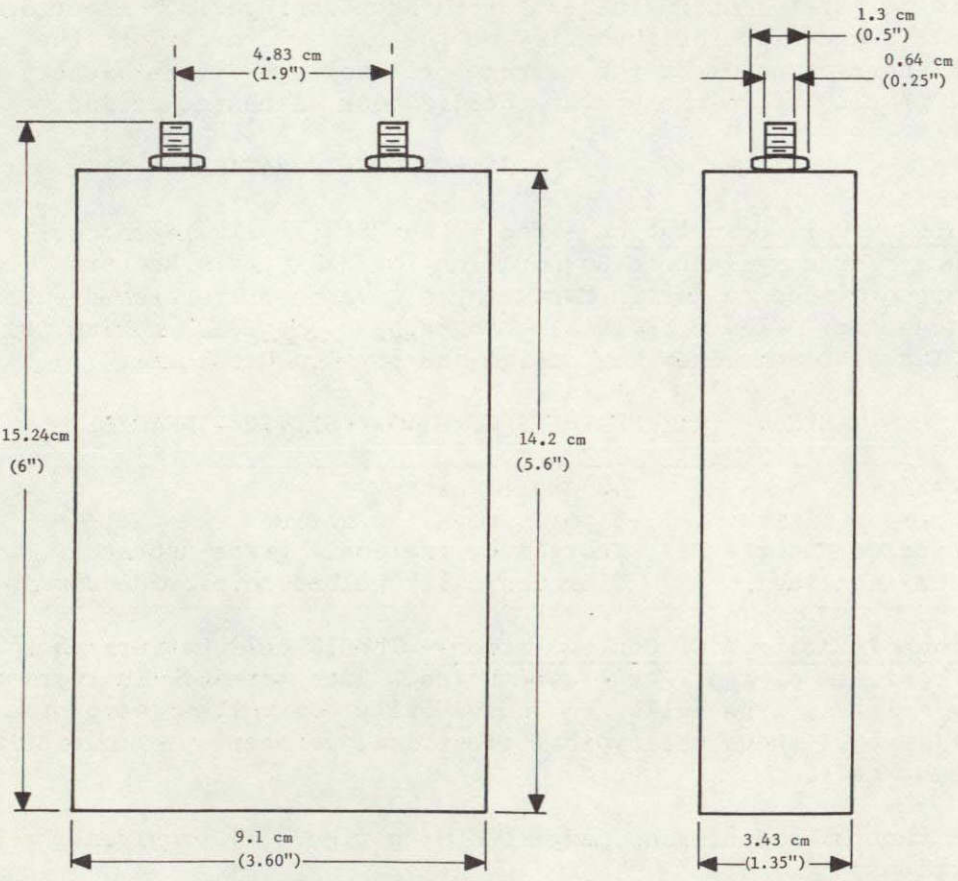


FIGURE 32 40-Ah SILVER-ZINC CELL, HS40-7,
WITH INORGANIC SEPARATOR

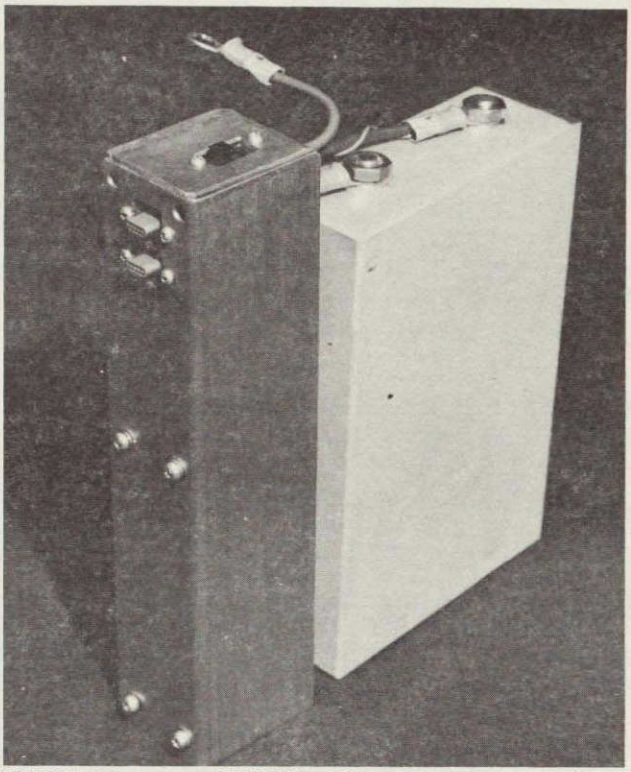


FIGURE 33 SINGLE CELL PROTECTOR (SCP) AND ONE 40-A h Ag-Zn CELL

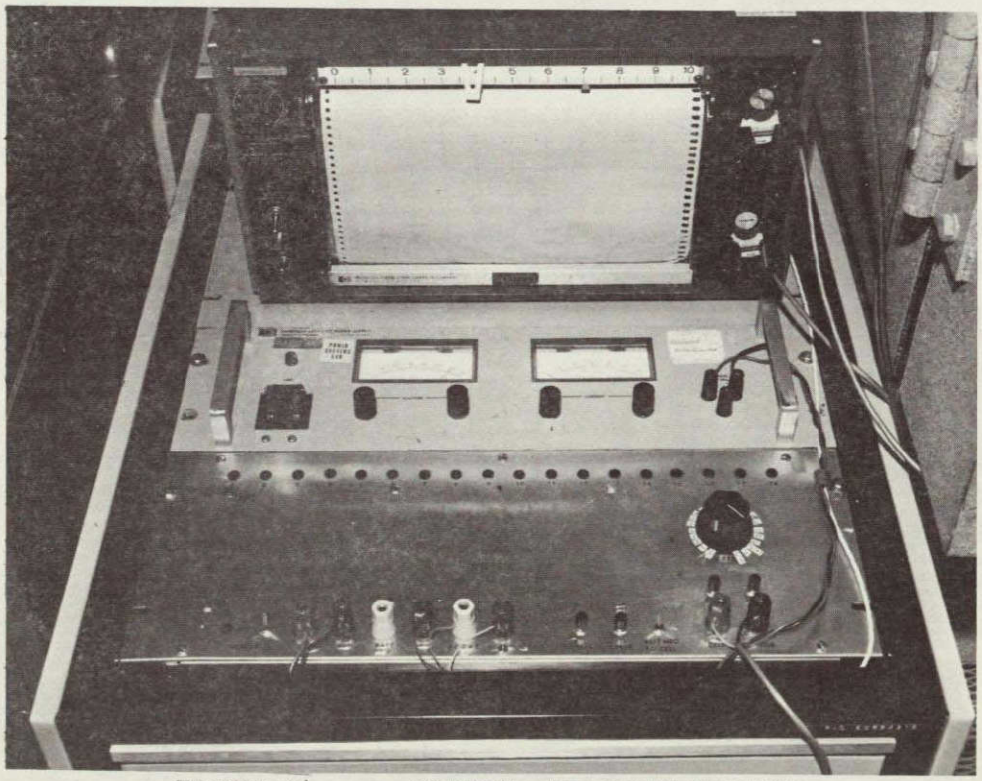


FIGURE 34 CONTROL AND DISPLAY PANEL

Set-reset of individual cells;
Set/reset of all cells;
Monitoring outputs for cell voltage and battery voltage;
Cell status lamp, on/off.

The test setup for group I assembly is shown in figure 35. In case of a failure by the SCP, automated Control and Data Acquisition System (ACDAS) automatically aborts the test and prints out which SCP failed. ACDAS control limits are the SCP voltage limits and function only in case of an SCP failure. Appendix A is a detailed description of the ACDAS.

3.2.3 Group II Battery/ACDAS Configuration - The Group II battery also contained 18 cells and was assembled in the same manner as the Group I configuration. Figure 36 shows the physical arrangement of the assembly and block diagram of the test setup. ACDAS provided the charge/discharge protection at the battery level.

3.2.4 Group III Cell/ACDAS, Voltage/Pressure Configuration - Two cells each equipped with pressure transducer and gage, were subjected to the 24-hour orbit cycle test to determine the effects of cycling on internal cell pressure. This test was not a part of the Task II objectives but was added to verify the adequacy of the selected charge control voltage limit. Figure 37 shows the test setup for the two cells. Removal of the cell from charge is accomplished by either a cell voltage or pressure limit signal by the ACDAS.

In addition to the SCP reset command capability of the C&D panel, ACDAS supplies a signal upon entering the charge phase, which resets all cell bypass relays, thus ensuring that all cells are connected in series at the start of each cycle.

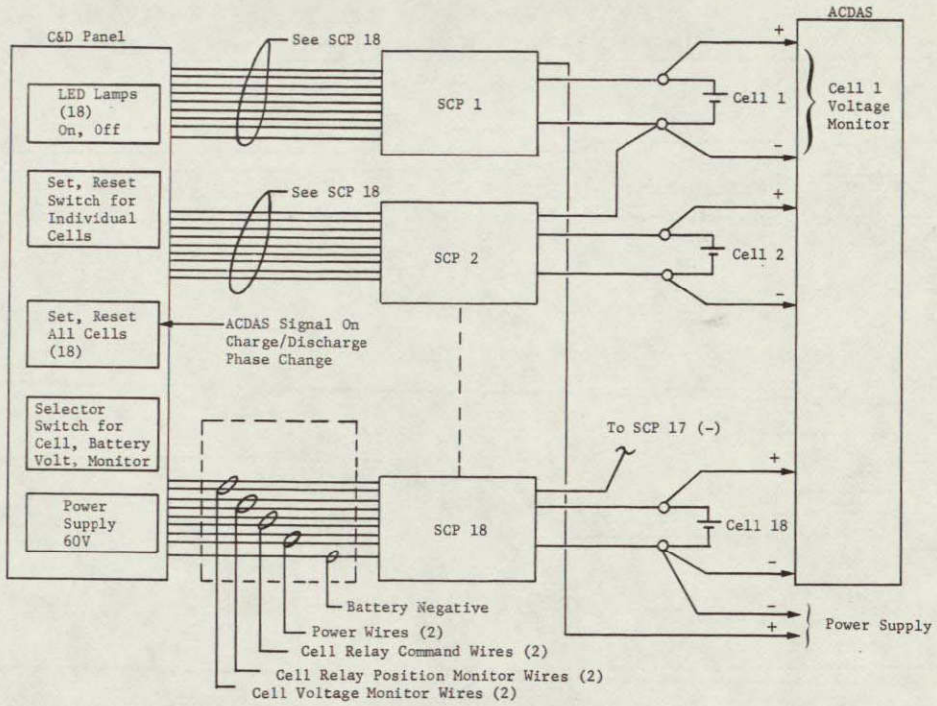
3.3 TEST PROCEDURE

3.3.1 Cell Matching - Forty-eight cells were subjected to two matching cycles at 22°C before assembly of the two battery groups. Matching cycle parameters were the same as those of postmanufacturing formation and acceptance test by Yardney Electric Corporation. The same criteria were used to ensure identical conditions in evaluating possible cell capacity degradation from the time of cell manufacture.

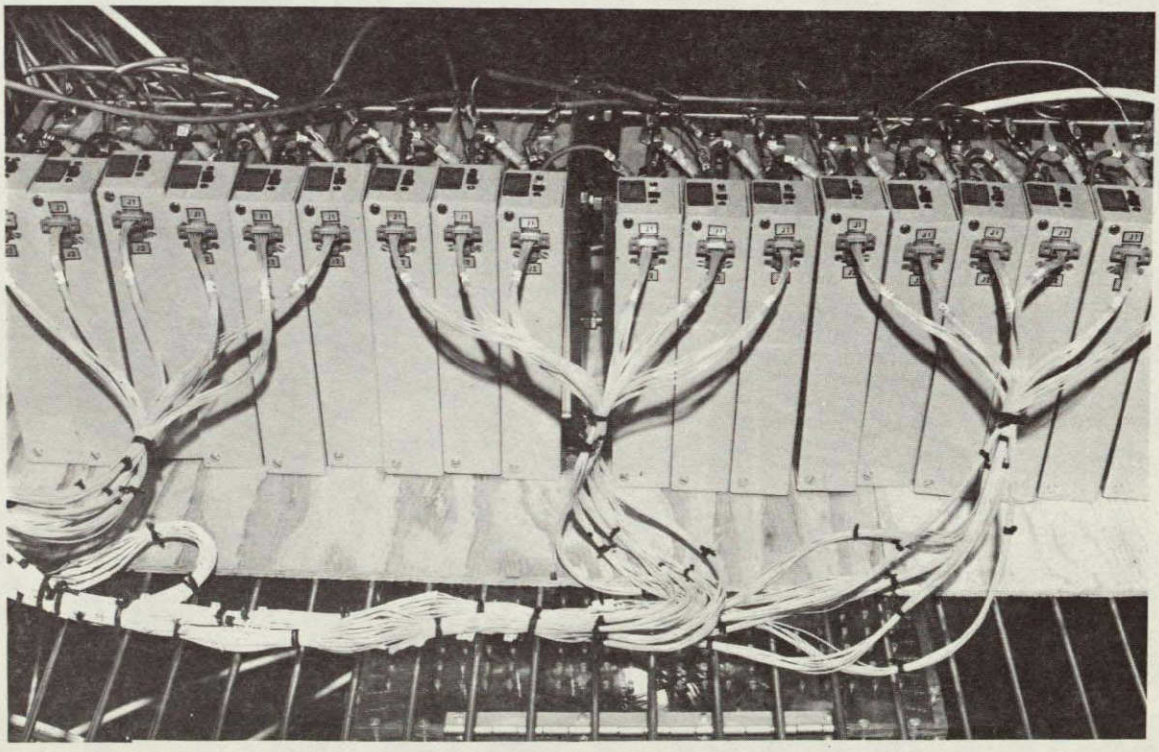
The matching cycle consisted of charging the cells at a 1.5-A rate to a cell voltage of 2.00 V/Cell or until 45-Ah input, whichever occurred first. This was followed by a discharge at a 6.0-A rate to a cell voltage of 1.0 V. An additional discharge was then made at a 3.0-A rate to 1.0 V/cell.

This test was performed using the laboratory automated control and data acquisition system (ACDAS).

3.3.2 Group I and II Battery Test - Both Group I and II batteries were subjected to identical simulated synchronous orbit (24 hours) cycling at 22°C. Control levels for these batteries are listed in Table 5.

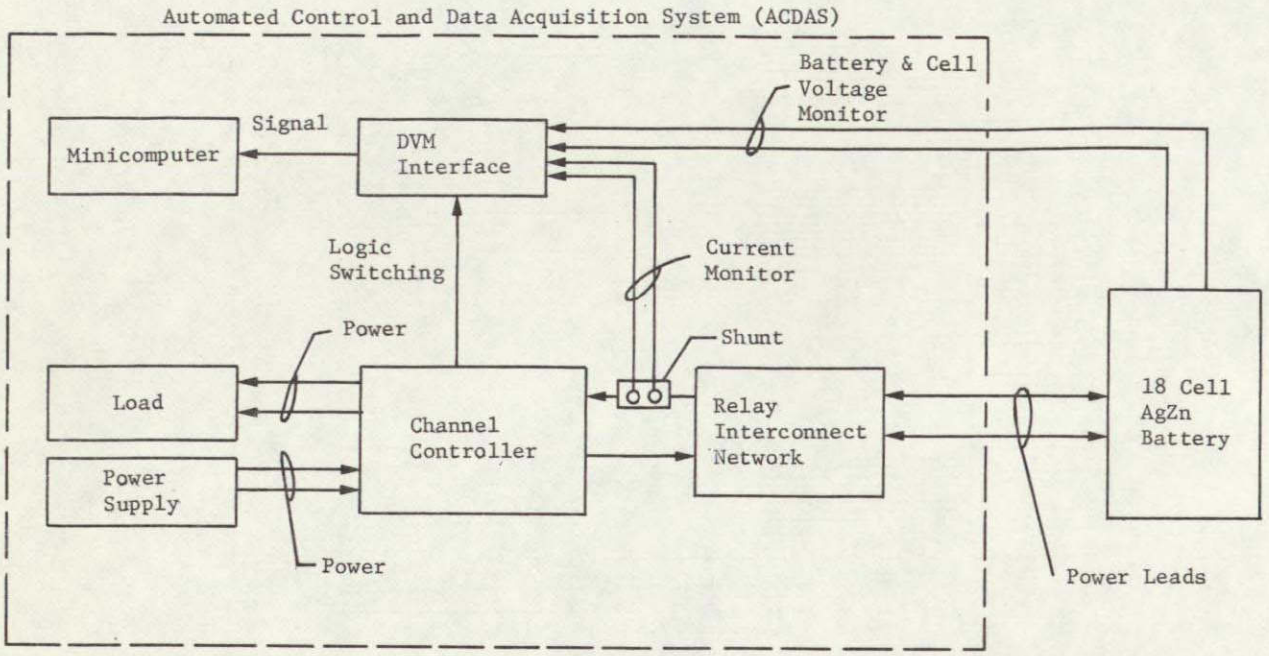


Functional Block Diagram

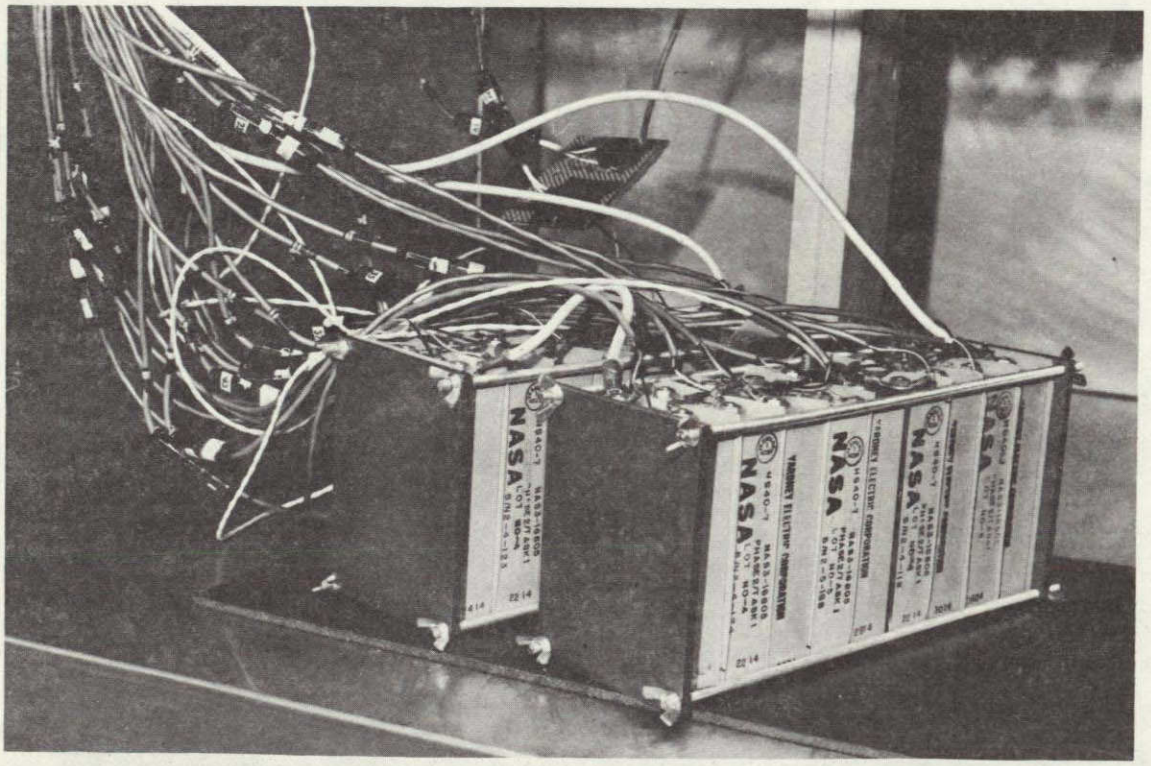


Group I Battery and SCPs in Test Chamber

FIGURE 35 TEST SETUP FOR SCP/GROUP I BATTERY

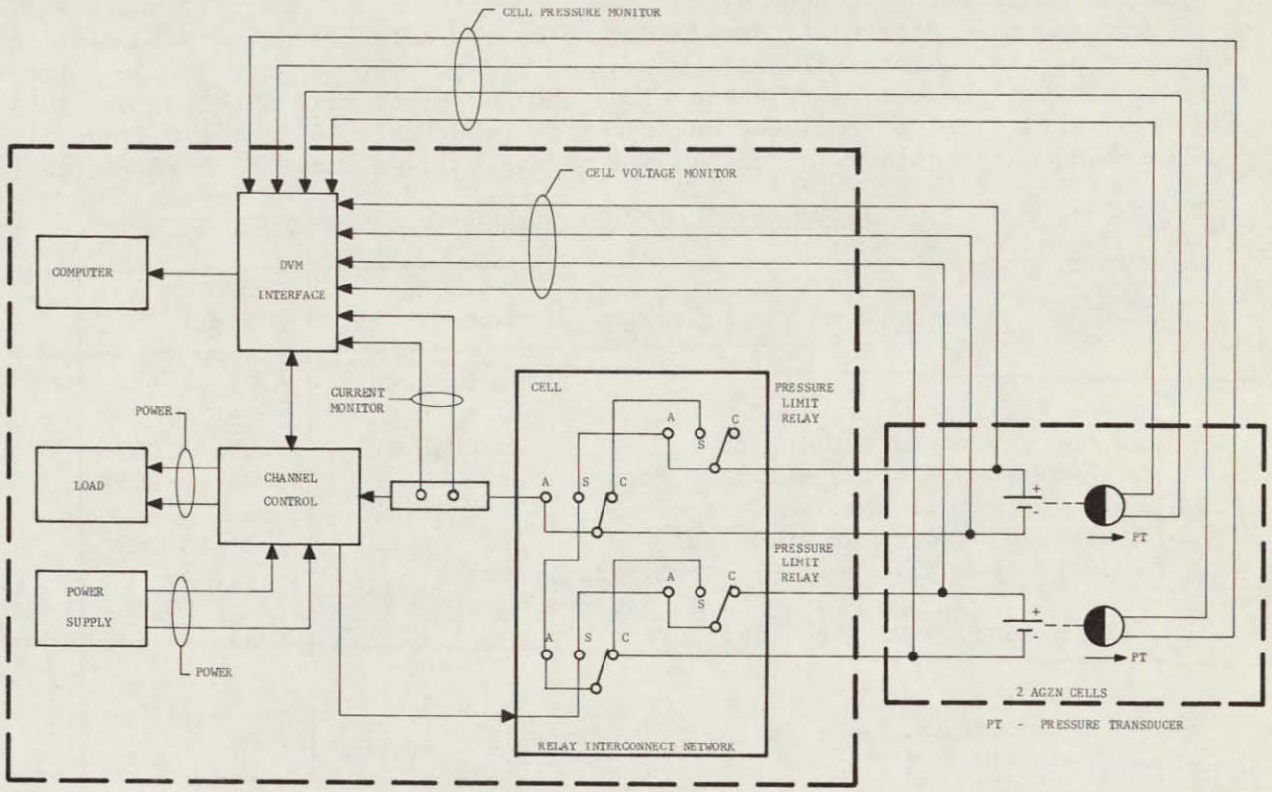


Functional Block Diagram

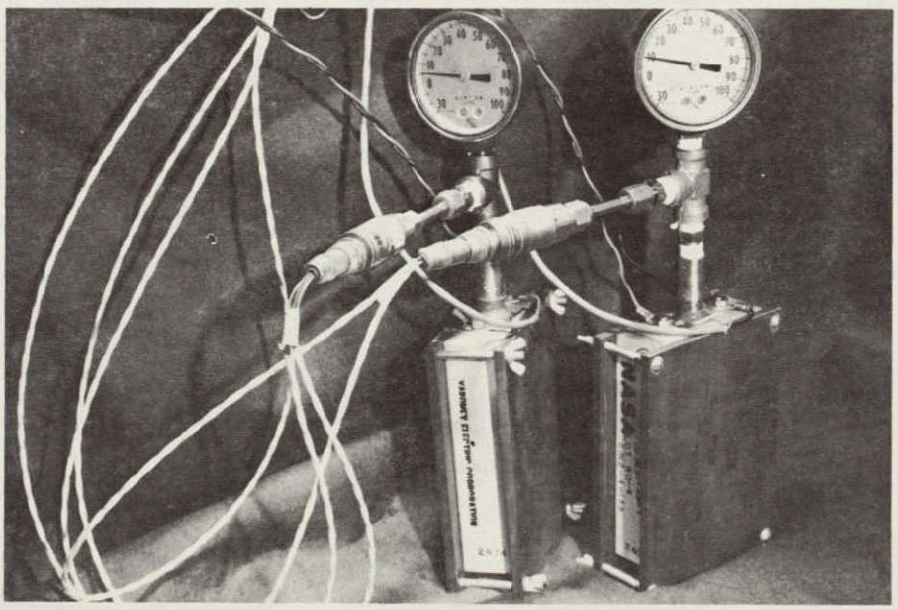


Group II Battery in Temperature Chamber

FIGURE 36 GROUP II BATTERY/ACDAS TEST SETUP



Functional Block Diagram



2 Cells (Group III) Used to Determine Effects of Cycling and Charge Voltage Limit on Cell Pressure

FIGURE 37 TEST SETUP FOR GROUP III CELLS

Both batteries were operated at 40% depth of discharge. The cell voltage limit of 1.98 Vdc was empirically determined to be the safe charge cutoff point to prevent excessive internal cell pressure buildup. The battery charge voltage limit was selected to be 1.98 Vdc times the number of series cells, or 35.64 Vdc. The first 12 cycles were conducted at 2.00-Vdc/cell charge voltage limit. All subsequent cycling was done at the charge voltage limit of 1.98 Vdc/cell.

TABLE 5 TEST PARAMETERS AND CONDITIONS FOR TWO BATTERY GROUPS

Control parameters	Group I Battery	Group II Battery
Charge rate, A	0.75 ±0.03	0.75 ±0.03
Discharge rate, A	13.3 ±0.03	13.3 ±0.03
Battery charge duration, hr	22.8 ±0.003	22.8 ±0.003
Battery charge voltage limit, Vdc	None	35.64 ±0.005
Cell charge voltage limit, Vdc	1.98 ±0.003	None
Battery discharge duration, hr	1.2 ±0.003	1.2 ±0.003
Battery discharge voltage limit, Vdc	None	22.5 +0 -0.005
Cell discharge voltage limit, Vdc	1.25 +0.005 -0	None
Cell discharge abort, Vdc	1.0 +0 -0.005*	None
Cell charge abort, Vdc	2.05 +0.005* -0	None
Temperature	22 ±3°C	22 ±3°C

*These are outside the SCP limits and are used only in the event of SCP failure(s).

Both batteries were operated in the latching mode, i.e., charge was terminated whenever the specified voltage limit was reached.

The following data were acquired and stored on the ACDAS magnetic tape:

1) Battery voltage;
2) Battery current;
3) Cell voltage;
4) Battery temperature;
5) Number of cycles.

Battery data were automatically recorded every 10 min during charge and every 5 min during discharge. In addition, the end of charge and discharge voltages were recorded.

3.3.3 Group III Battery Test - The two pressure-instrumented cells comprising the Group III pack were subject to nearly the same cycling parameters as Groups I and II. The main difference was that the charge voltage limit was varied during the cycling test to determine the effects of various voltage limits on internal cell pressure. Table 6 shows the cycles in which charge voltage limits were adjusted.

TABLE 6 CHARGE VOLTAGE LIMIT VERSUS CYCLE

Cycle No.	Cell charge voltage limit setting, Vdc
1 to 14	2.00
15 to 28	2.05
29 to 45	2.10
46 to present*	2.00

*As of April 18, 1976, the cutoff date for this report, 110 cycles have been completed.

The effects of aging on internal cell pressure at various charge voltage limits will be investigated during Phase II of this program (April 19, 1976 through April 18, 1977).

3.4 FAILURE AND TEST CONTINUATION CRITERIA FOR GROUPS I AND II

Test failure is the point where all cells in the batteries will not perform within the limits of the test regime. As failure of a cell occurs, that cell will be removed and the test continued until the end of the contract period. For the SCP controlled battery the bypass circuit shall provide the necessary bypass function in case of the cell failure. When any anomaly or failure occurs, the LeRC project manager will be contacted within one working day after its occurrence. Any changes to the test condition or configuration will be verbally coordinated and approved by the LeRC project manager or his representative before implementing the changes and continuing the test.

3.5 RESULTS AND DISCUSSION

3.5.1 Cell Matching - Table 7 summarizes the capacity obtained for the 48 cells. Figure 38 shows the capacity distribution of the cells plotted on statistical probability graph paper. When data are plotted on this paper, statistical parameters such as standard deviation and mean value can be readily obtained.

The average capacity of 48 cells was 40.5 Ah, with a standard deviation in capacity of 0.65 Ah. The total capacity dispersion was a maximum of 2.15 Ah.

Table 8 lists the average capacity obtained at Martin Marietta and YEC. Figure 39 graphically illustrates the comparison of these data.

TABLE 7 CAPACITY DATA FOR CELL MATCHING TEST

Cell S/N	Cycle 1, Ah	Cycle 2, Ah	Avg. cap., Ah	Battery Test Group
4-108	39.833	43.267	41.550	
4-113	39.833	43.185	41.509	
4-136	39.833	42.919	41.376	
4-134	39.833	42.769	41.301	
4-131	39.833	42.703	41.268	
4-127	39.833	42.637	41.235	
4-132	39.833	42.504	41.169	
4-137	39.833	42.354	41.094	
5-162	39.833	42.188	41.011	
4-121	39.833	42.121	40.977	Group I
5-146	39.833	41.855	40.844	
4-133	39.833	41.838	40.836	
5-163	39.833	41.672	40.753	
4-111	39.833	41.655	40.744	
4-116	39.833	41.605	40.719	
4-119	39.833	41.555	40.694	
5-165	39.833	41.539	40.686	
4-107	39.833	41.539	40.685	
5-158	39.833	40.572	40.203	
5-164	39.800	40.539	40.170	
4-130	39.833	41.522	40.678	
5-160	39.833	41.522	40.678	
4-117	39.833	41.456	40.645	
4-120	39.833	41.356	40.595	
5-147	39.833	41.356	40.595	
4-109	39.833	41.289	40.561	
4-115	39.833	41.141	40.487	
4-123	39.833	41.122	40.478	
4-125	39.833	41.072	40.453	Group II
4-135	39.833	41.038	40.436	
4-124	39.833	40.989	40.411	
5-167	39.833	40.989	40.411	
5-166	39.833	40.956	40.394	
5-161	39.833	40.922	40.378	
4-118	39.833	40.806	40.320	
5-171	39.833	40.706	40.270	
5-149	39.833	40.656	40.245	
4-126	39.833	40.639	40.236	
5-173	39.833	40.489	40.161	
4-122	39.833	40.205	40.019	
5-148	39.833	40.039	39.936	
5-159	39.715	40.039	39.877	Group IV*
5-169	39.443	40.172	39.808	
5-156	39.833	39.705	39.769	
5-172	39.833	39.621	39.727	
5-157	39.359	40.089	30.720	
4-112	39.833	39.421	39.627	
4-129	39.833	39.021	39.427	

*Microprocessor-controlled pack, See Section 4.4

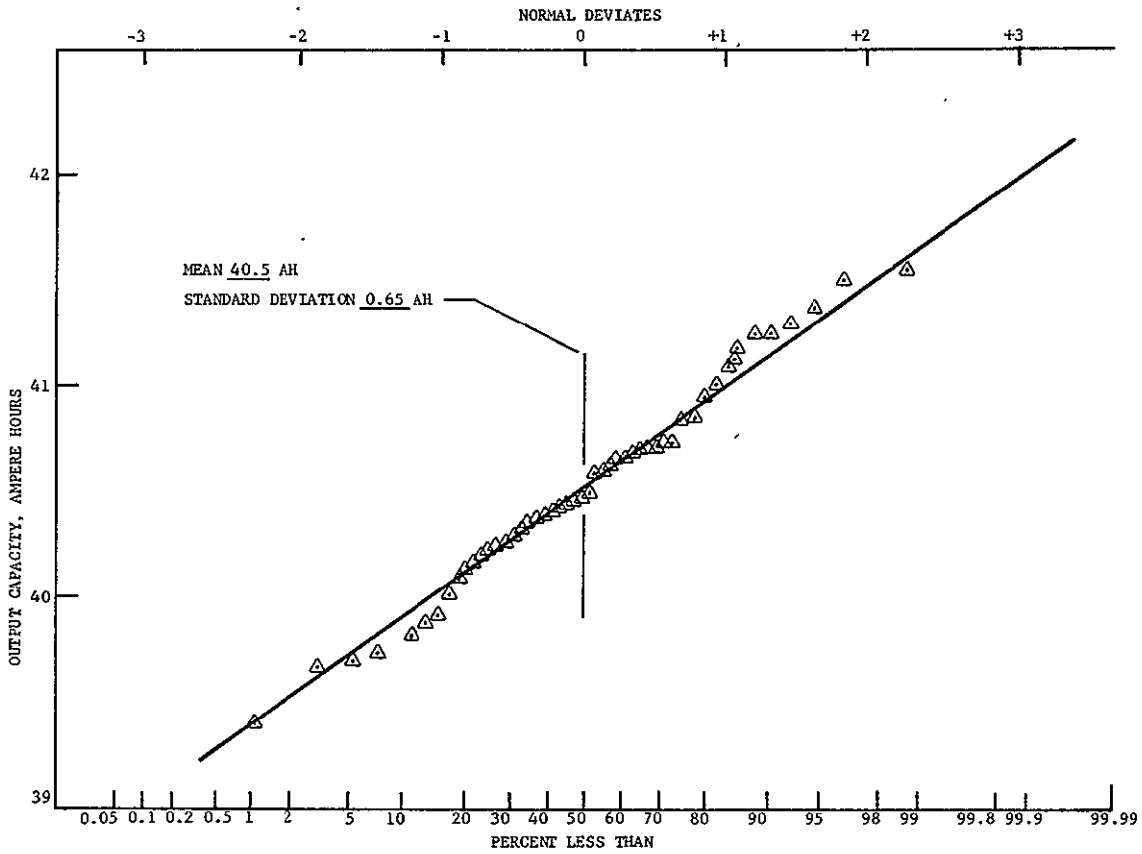


FIGURE 38 CAPACITY DISTRIBUTION OF 48 CELLS, CELL MATCHING TEST

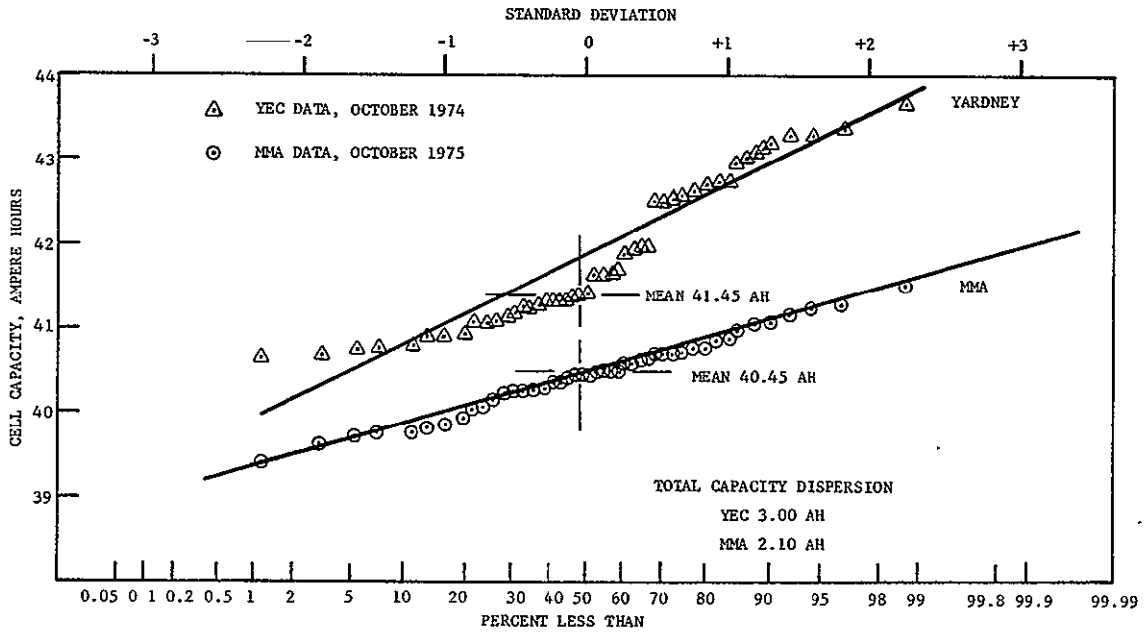


FIGURE 39 COMPARISON OF YARDNEY AND MARTIN MARIETTA CAPACITY DATA ON 48 CELLS

TABLE 8 CAPACITY DATA, MARTIN MARIETTA AND YARDNEY ON 48 CELLS

Cell S/N	Martin Marietta Average Capacity, Ah October 1975	Yardney Capacity, Ah October 1974	Battery Test Group
4-108	41.550	42.53	
4-113	41.509	43.09	
4-136	41.376	43.36	
4-134	41.301	43.06	
4-131	41.268	43.18	
4-127	41.235	42.71	
4-132	41.169	42.96	
4-137	41.094	43.29	Group I
5-162	41.011	41.29	
4-121	40.977	41.10	
5-146	40.844	41.36	
4-133	40.836	43.135	
5-163	40.753	41.29	
4-111	40.744	41.87	
4-116	40.719	40.92	
4-119	40.694	40.80	
5-165	40.686	41.17	
4-107	40.685	42.04	
5-158	40.203	42.59	Spare
5-164	40.170	40.99	Spare
4-130	40.678	42.75	
5-160	40.678	41.35	
4-117	40.645	40.77	
4-120	40.595	41.40	
5-147	40.595	41.47	
4-109	40.561	42.59	
4-115	40.487	42.51	Group II
4-123	40.478	41.92	
4-125	40.453	41.99	
4-135	40.436	43.06	
4-124	40.411	41.99	
5-167	40.411	40.92	
5-166	40.394	41.02	
5-161	40.378	40.79	
4-118	40.320	40.66	
5-171	40.270	41.40	
5-149	40.245	41.59	
5-126	40.236	42.760	
5-173	40.161	41.33	
5-122	40.019	41.323	
5-148	39.936	41.59	
5-159	39.877	41.69	Group IV
5-169	39.808	40.69	
5-156	39.769	41.65	
5-172	39.727	41.45	
5-157	39.720	41.29	
4-112	39.627	43.28	
4-129	39.427	42.73	

The mean capacity degradation the 48 cells in 12 months of activated life was 1.0 Ah. Note in figure 39 that Martin Marietta data show less capacity dispersion among the 48 cells than Yardney Electric data.

Two 18-cell battery groups were selected from this 48-cell lot. Selection of the cells was based on the closest grouping in capacity. Group I battery cell capacity ranged from 40.68 to 41.55 Ah. Group II battery cell capacity ranged from 40.22 to 40.69 Ah. These data are plotted in figure 40 and 41, respectively.

Cell matching test conditions were identical to those of Yardney Electric Corporation (YEC) during their postmanufacturing formation and acceptance test. The secondary objective of the matching test was to determine the extent of possible cell degradation by comparing the capacity data obtained by YEC in October 1974 and Martin Marietta in October 1975.

3.5.2 Group I Battery/SCP Test - A total of 110 cycles have been completed as of April 18, 1975 on the SCP-controlled battery assembly without failure of the SCP or the cells. Figure 42 is a plot of the average end of charge voltage. Although the cells were initially fully charged (45-Ah input), it required 12 full cycles before all cells reached the voltage limit. During the first 12 cycles, the cells operated under an average ampere-hour recharge fraction (RF) of 1.07. The voltage limit of each SCP was adjusted at this point to a limit of 1.98 V/cell. This change was the result of pressure data obtained in Group III testing, which indicated that 1.98 Vdc/cell will prevent pressure buildup in a cell. Operating at the 1.98-Vdc limit resulted in an ampere-hour RF of 1.02. Again, 12 full cycles were required before the cells reached the 1.98 voltage limit. Voltage limiting has continued through 100 cycles of operation, indicating that the SCPs are functioning properly.

Figure 43 shows the deviation for the Group I battery. The large deviation during the early cycles (1 to 12) is mainly attributed to the higher voltage limit of 2.00 Vdc and the fact that only a few cells reached the voltage limit during this time.

Figure 44 shows the average end of discharge (EOD) voltage for the cells. Cell voltage stabilization was achieved through the first 10 cycles of operation (2.0-Vdc limit), with a slight voltage decay evidence in cycles 11 and 12. After readjustment of the charge voltage limit to 1.98 Vdc, the EOD voltage again increased until it stabilized, then began to degrade. The degradation followed a trend similar to that of the 2.00-Vdc charge voltage limit. The slope of the EOD voltage curve is 4.1×10^{-4} V/cycle between 20 and 100 cycles. The linearity of the data on a semilogarithmic chart indicates that the EOD voltage decays exponentially with cycles. It also indicates that the EOD trend line may be a good parameter for predicting cycle life at specific charge control and test conditions.

Figure 45 shows the end-of-discharge voltage dispersion. It can be seen that the EOD voltage spread generally increases with cycling.

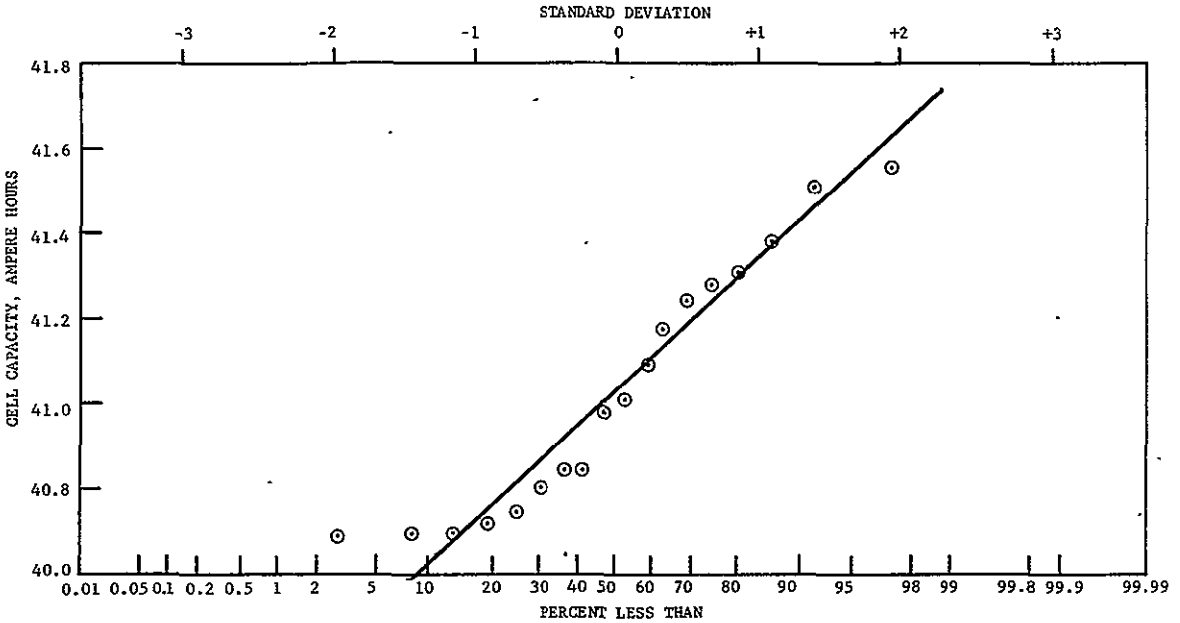


FIGURE 40 GROUP I BATTERY CELL CAPACITY DISTRIBUTION

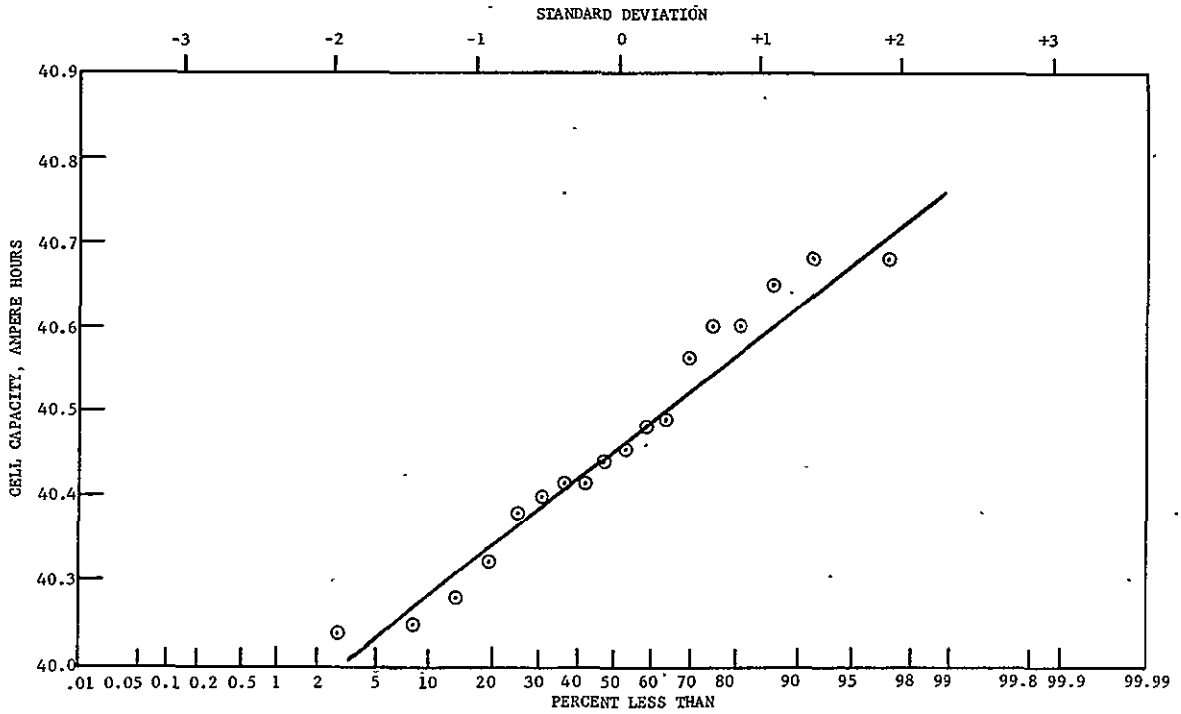


FIGURE 41 GROUP II BATTERY CELL CAPACITY DISTRIBUTION

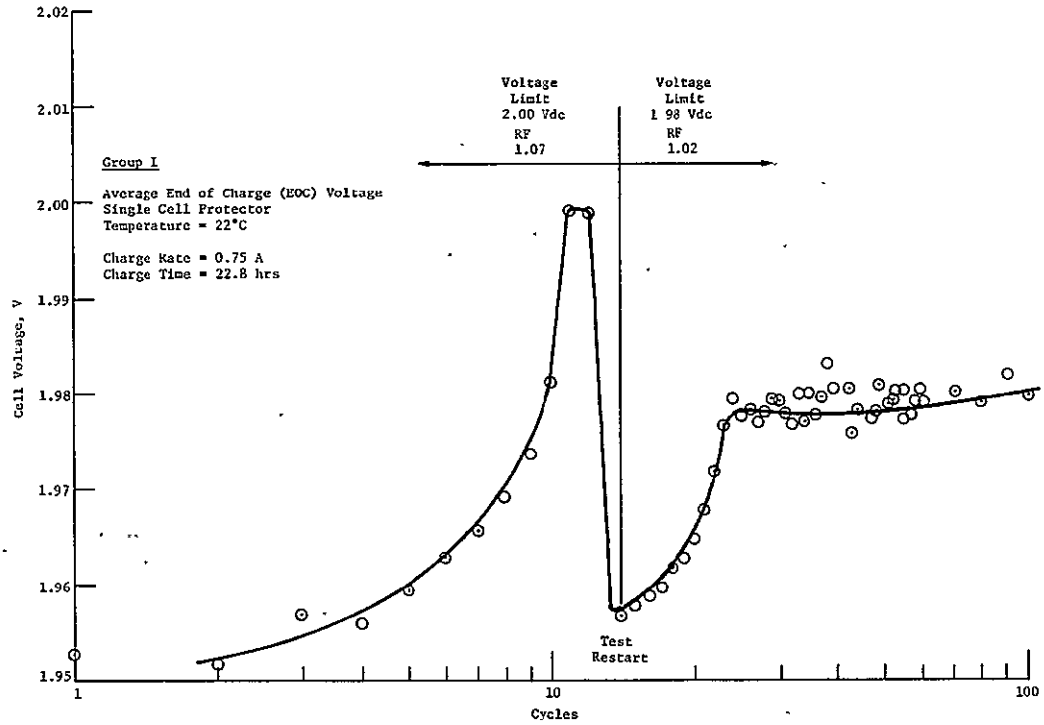


FIGURE 42 AVERAGE END OF CHARGE VOLTAGE FOR CELLS IN GROUP I

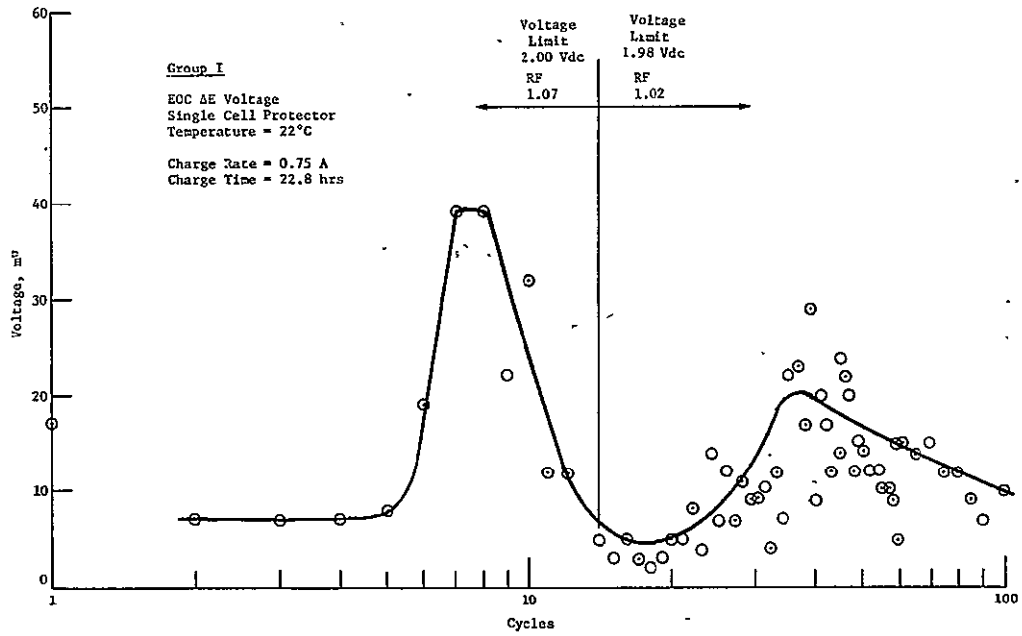


FIGURE 43 MAXIMUM CELL EOC VOLTAGE DEVIATION FOR CELLS IN GROUP I BATTERY

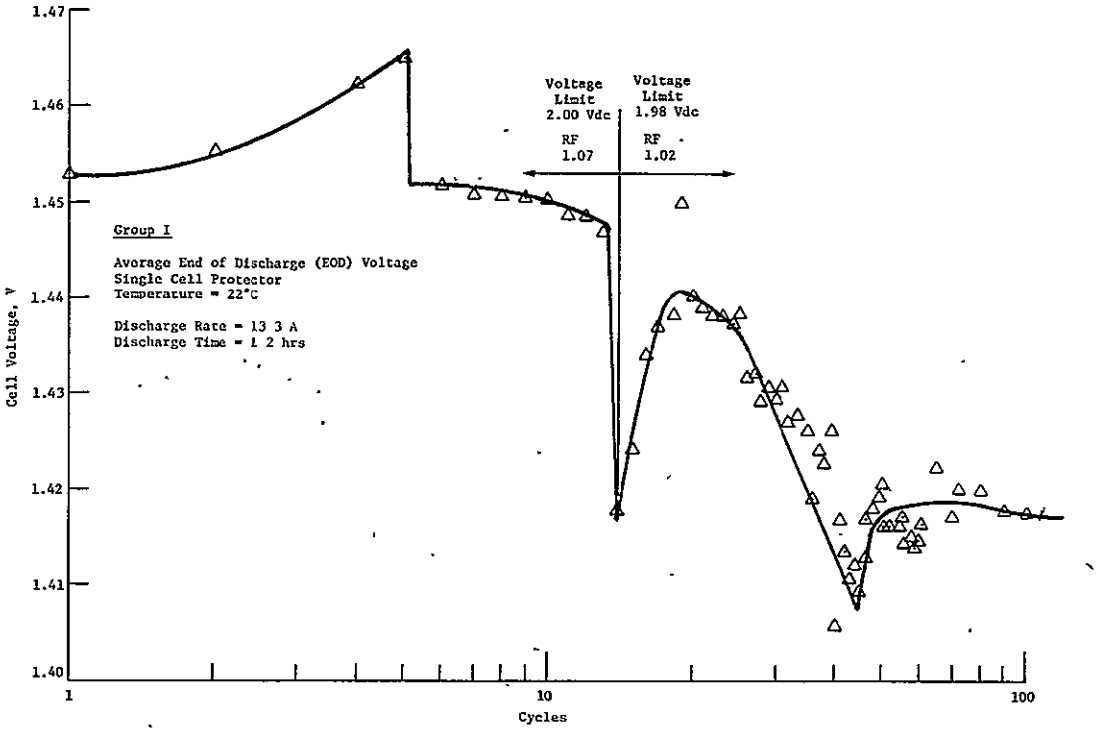


FIGURE 44 END OF DISCHARGE CELL VOLTAGE FOR GROUP I BATTERY

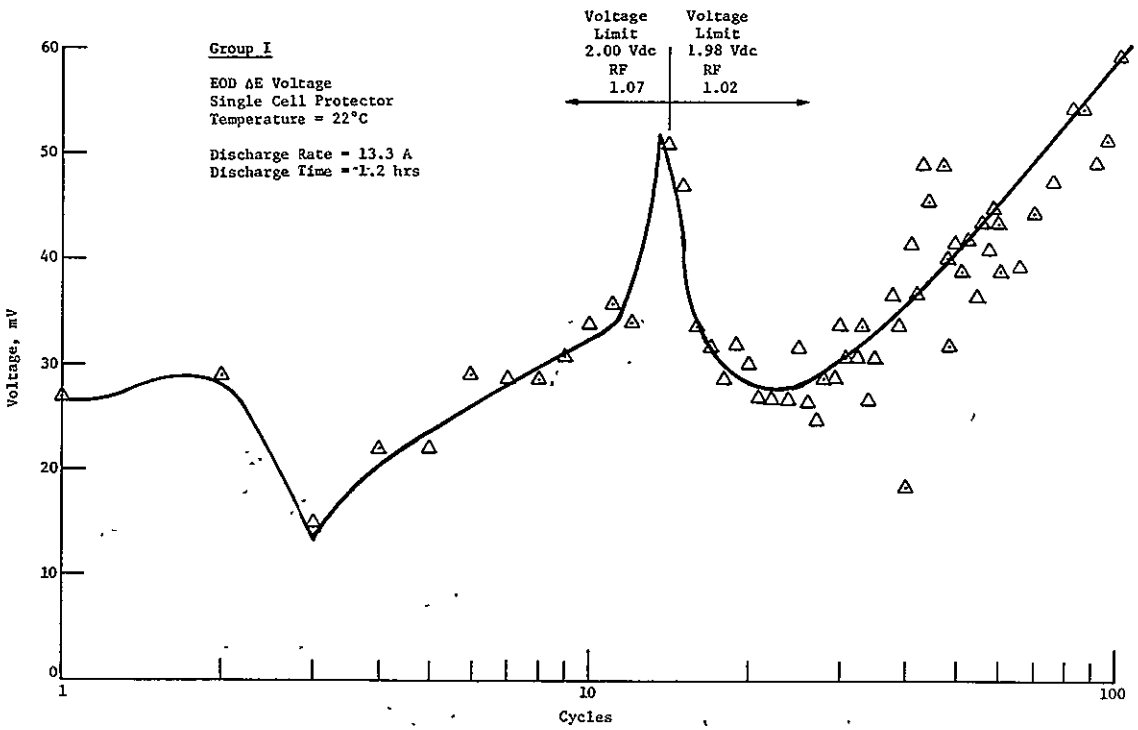


FIGURE 45 MAXIMUM CELL EOD VOLTAGE DISPERSION FOR GROUP I BATTERY

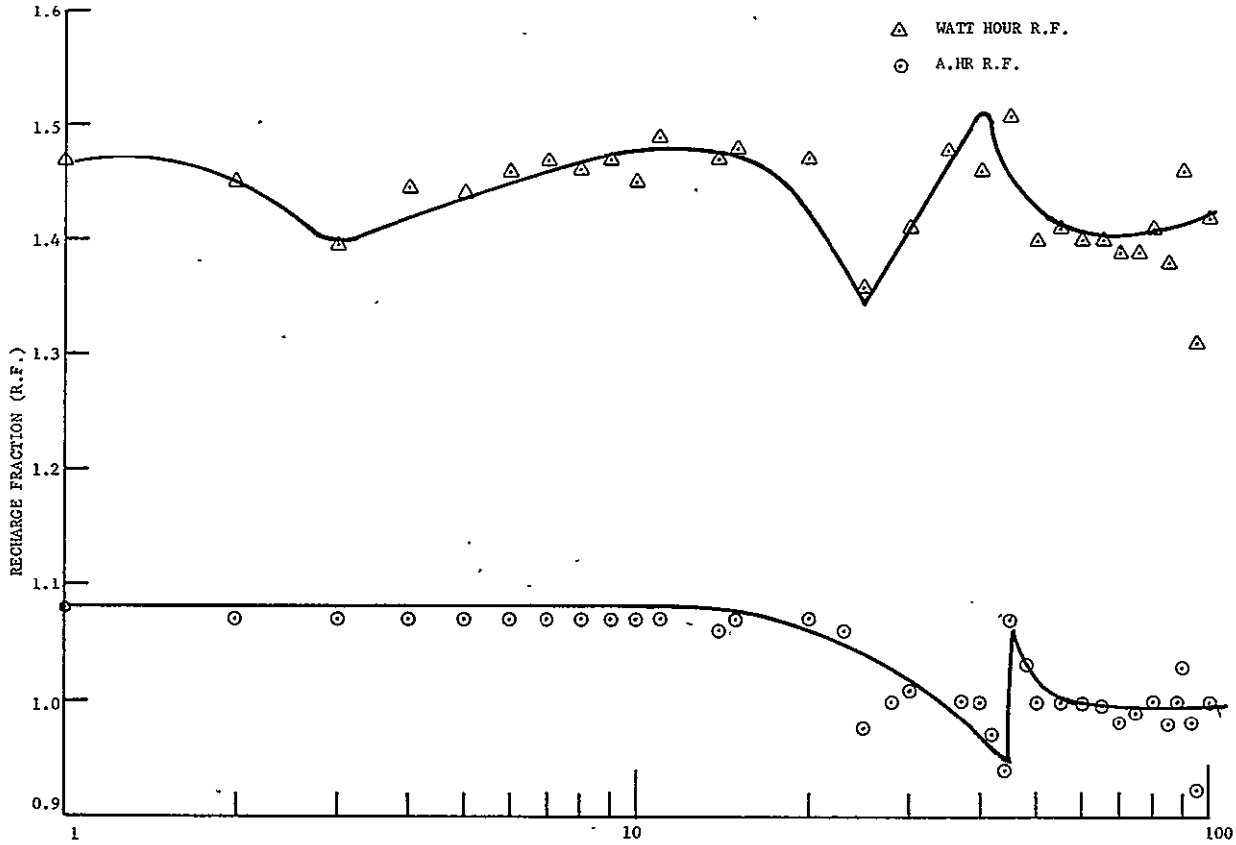


FIGURE 46 RECHARGE FRACTION FOR GROUP I BATTERY

Figure 46 shows the average ampere-hour and watt-hour recharge fraction (RF) for the cells in the Group I battery. During the first 12 cycles at the voltage limit of 2.00 Vdc, the average ampere-hour RF was 1.07. At the voltage limit of 1.98 Vdc, the RF was 1.02. This lower voltage limit may be inadequate to amintain proper energy balance in the cells. Figure 47 through 49 show typical charge/discharge voltage profiles from the cycle data obtained during Task II. As expected, the time required to reach the peroxide level decreases with cycling.

3.5.3 Group II Battery/ACDAS Test - The battery completed 110 cycles (as of April 18, 1976) without any abnormalities or failure. The first 12 cycles were conducted at a voltage limit of 36.0 Vdc, or an average of 2.0 Vdc/cell. As with the Group I test, the charge cutoff voltage was reduced to 35.64 Vdc (1.98 Vdc/cell) on the thirteenth cycle, and this limit was held constant through all subsequent cycles.

Figures 50 and 51 show the battery EOC voltage and maximum deviation in cell EOC voltages, respectively, as functions of cycle. During the first 10 cycles when the battery EOC voltage had not reached the cutoff point, the cell EOC voltage spread increased to 58 mV.

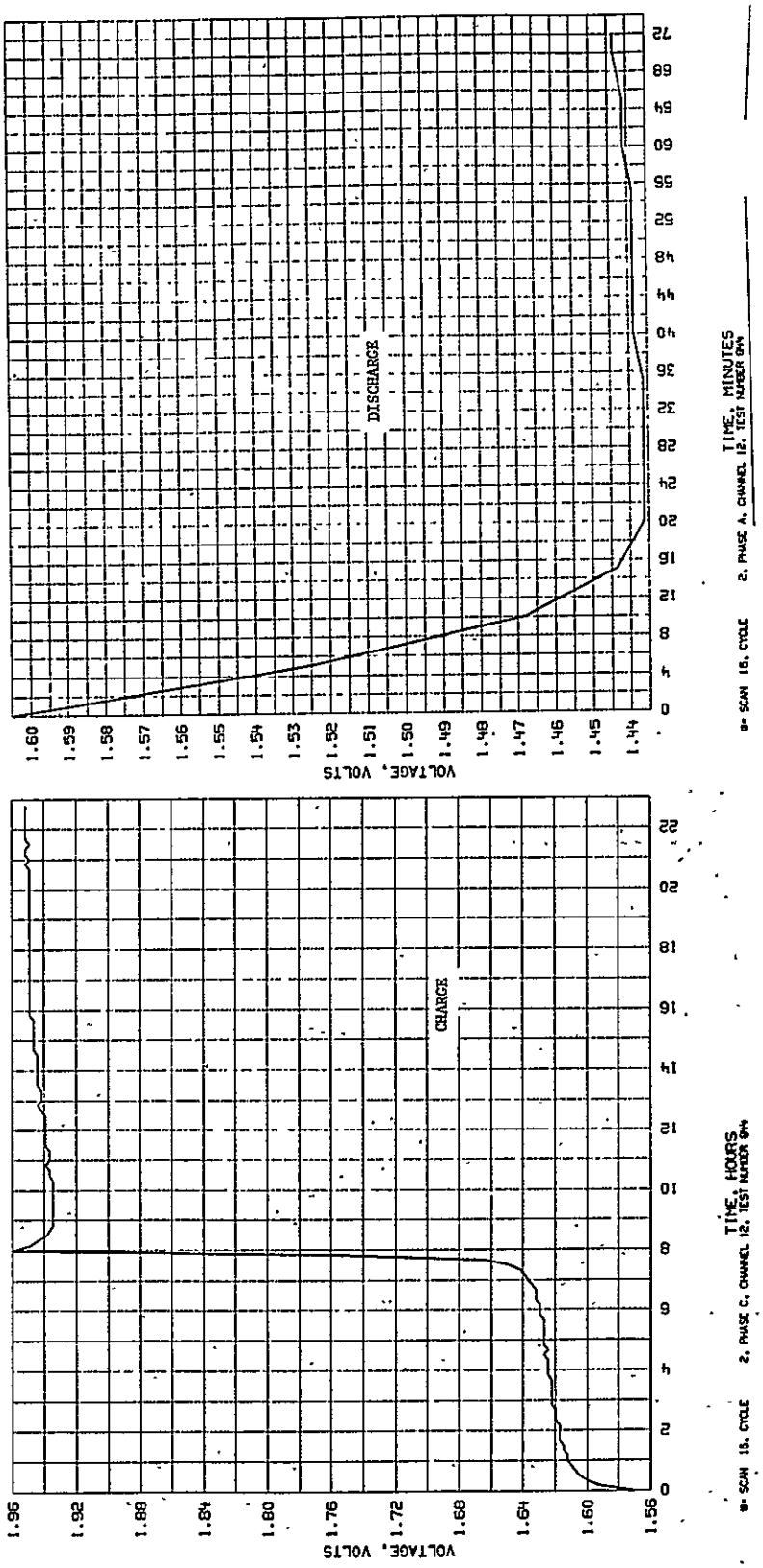


FIGURE 47 VOLTAGE PROFILE AT CYCLE NO. 1, GROUP I

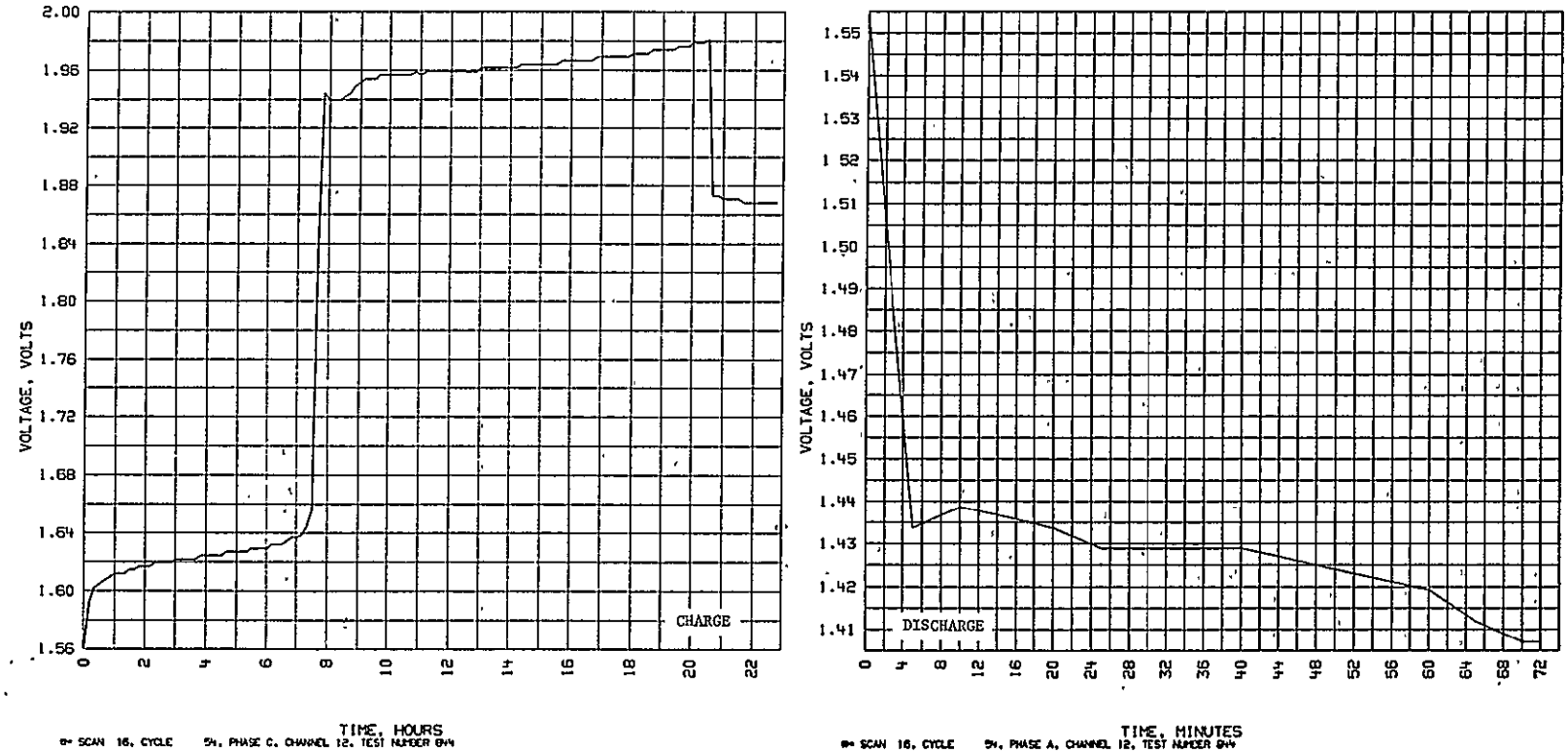


FIGURE 48 VOLTAGE PROFILE AT CYCLE NO. 54, GROUP I

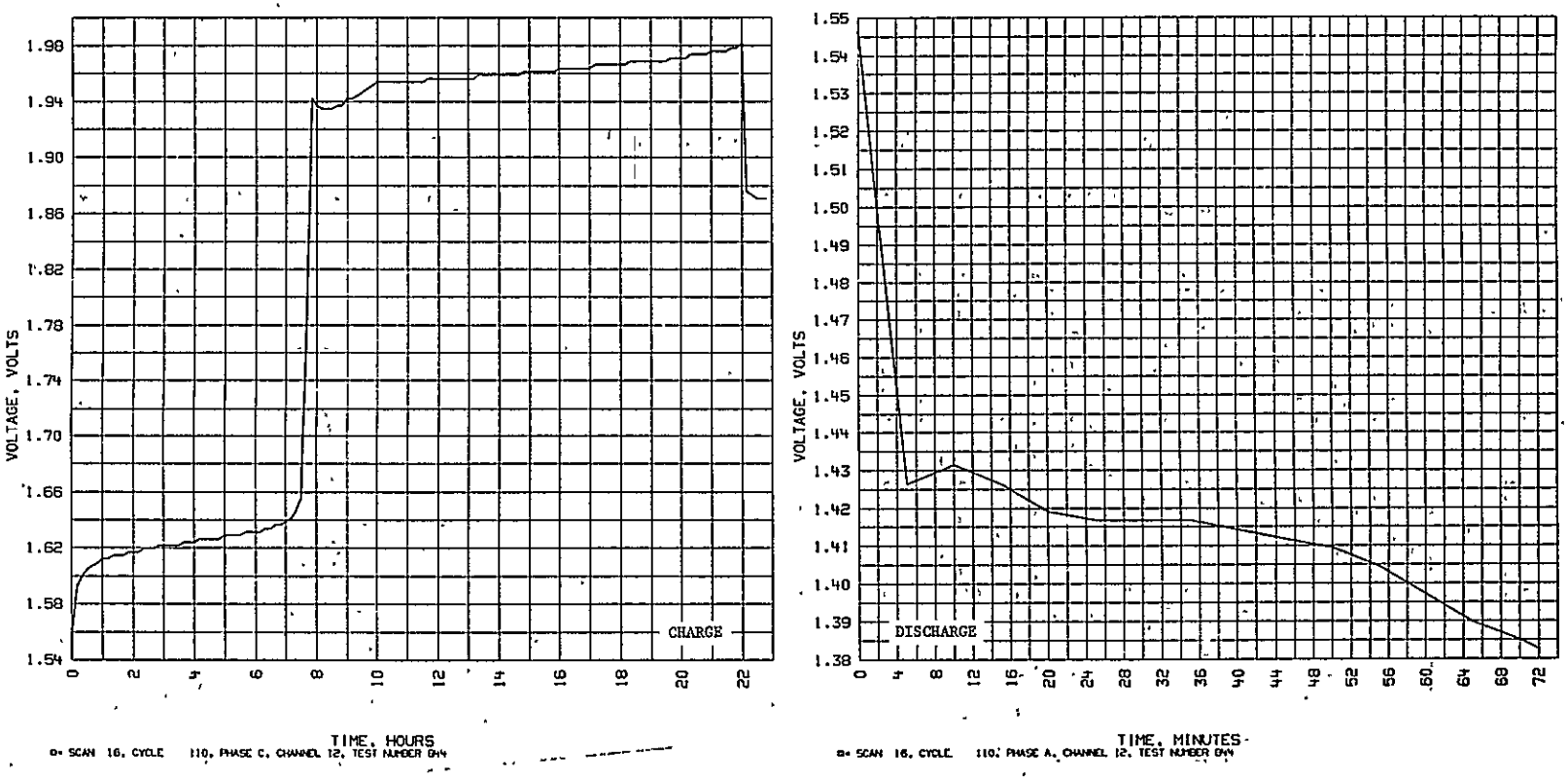


FIGURE 49 VOLTAGE PROFILE AT CYCLE NO. 110, GROUP I

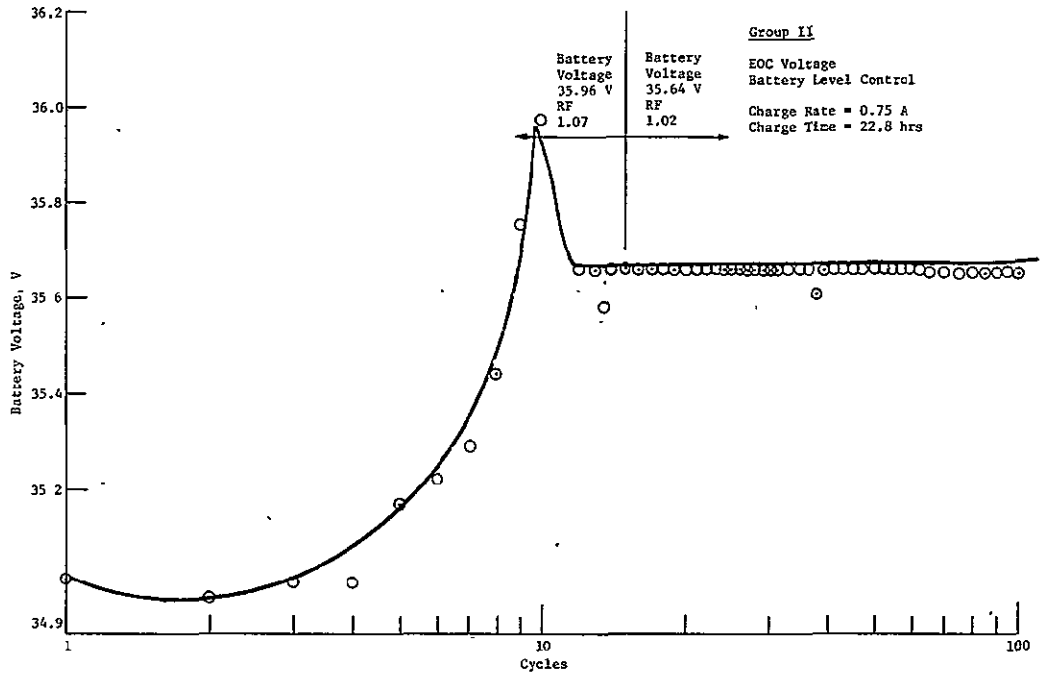


FIGURE 50 END OF CHARGE BATTERY VOLTAGE, GROUP II BATTERY

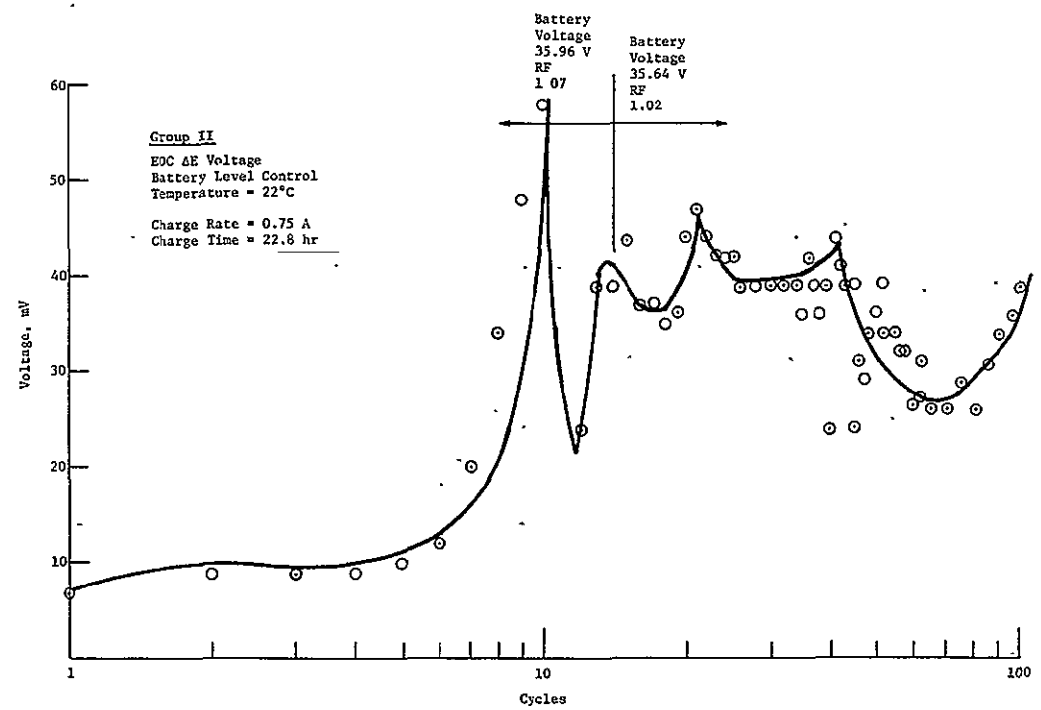


FIGURE 51 MAXIMUM EOC CELL VOLTAGE DEVIATION, GROUP II BATTERY

In each subsequent cycle from the twelveth cycle on, the battery voltage reached the limit of 35.64 Vdc and went to an open circuit condition for the remainder of the charge phase. During this time, the EOC cell voltage dispersion ranged between 20 and 47 mV, with an average of about 40 mV. Thus, cell voltage divergence can be reduced to some extent by reducing the battery charge voltage limit.

Figures 52 and 53 show the EOD voltage and maximum deviation in the cell EOD voltages, respectively, versus cycles. The degradation in the EOD voltage between 20 and 100 cycles is 6.8 mV/cycle for the battery or 3.8×10^{-4} V/cycle for the cells. As discussed earlier for the Group I battery, this degradation rate is affected to some extent by the amount of overcharge. Figure 54 shows both watt-hours and ampere-hour RF. The RF that represents the amount of overcharge in turn is controlled by the charge voltage limit used. For example, at 36.0-Vdc battery voltage limit (2.0 Vdc per cell), the ampere-hour RF was 1.07, and at a 35.64-Vdc limit (1.98 Vdc per cell), the ampere-hour RF remained between 0.975 and 1.04.

Typical voltage profiles are shown in figures 55 through 57 for cycles 1, 42, and 101, respectively.

3.5.4 Group III Battery/ACDAS Test - Pressure-transducer-mounted cells (S/N 4-138 and 4-139) were cycled under the same regime as Group I and II batteries, except for the charge voltage limit.

Figures 58 and 59 show the internal cell pressure at EOC and EOD versus cycle for the two cells. Typical cell voltage and pressure profiles are shown in figure 60.

The first 16 cycles were run at the charge voltage limit of 2.00 Vdc. The highest pressure appeared to have stablized at close to 34.5kPa (5 psig) after 9 cycles. The charge voltage limit was then increased to 2.05 Vdc on the 17th cycle. Both cells reached a stable pressure, with cell S/N 4-139 exhibiting the highest pressure at 93.2kPa (13.5 psig) (see figure 60).

On the 28th cycle, the charge voltage limit was further increased to 2.10 Vdc. Because cell pressure continued to increase on each subsequent cycle, the charge voltage limit was readjusted back to 2.0 Vdc. The cells were then cycled at this voltage limit for more than 50 cycles without causing any pressure increase.

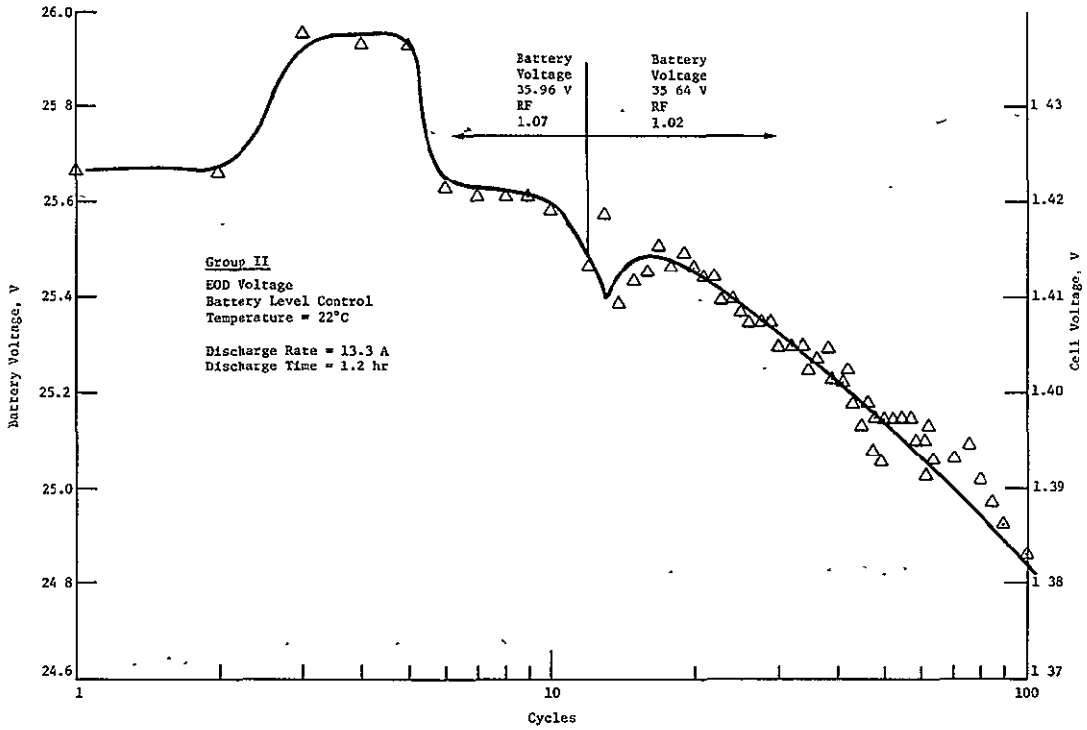


FIGURE 52 END OF DISCHARGE VOLTAGE OF CELLS IN BATTERY, GROUP II

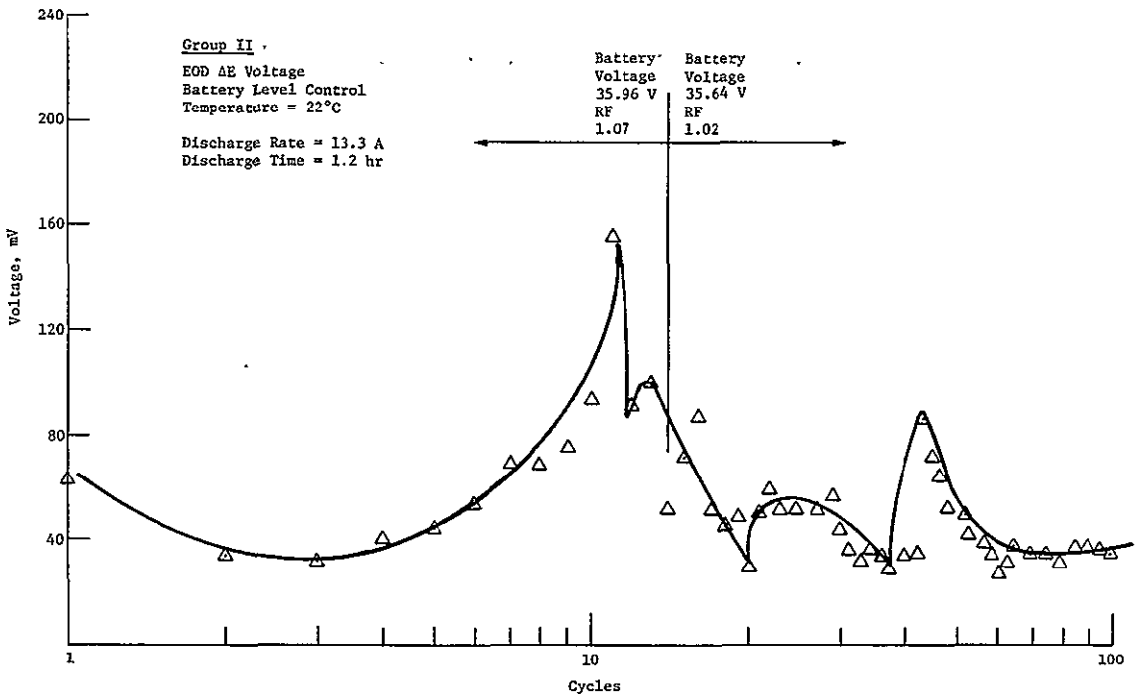


FIGURE 53 MAXIMUM DEVIATION IN END OF DISCHARGE VOLTAGE OF CELLS IN BATTERY, GROUP II

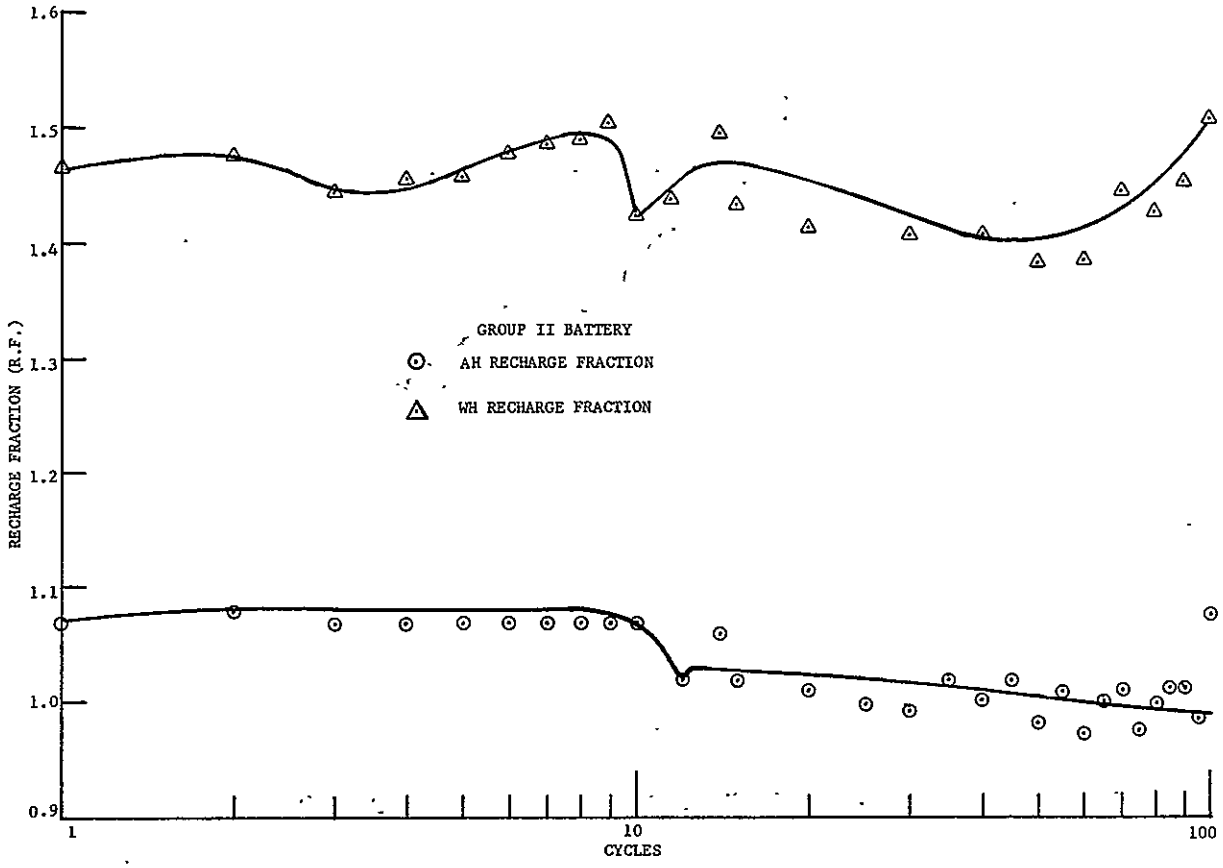


FIGURE 54 RECHARGE FRACTION FOR GROUP II BATTERY

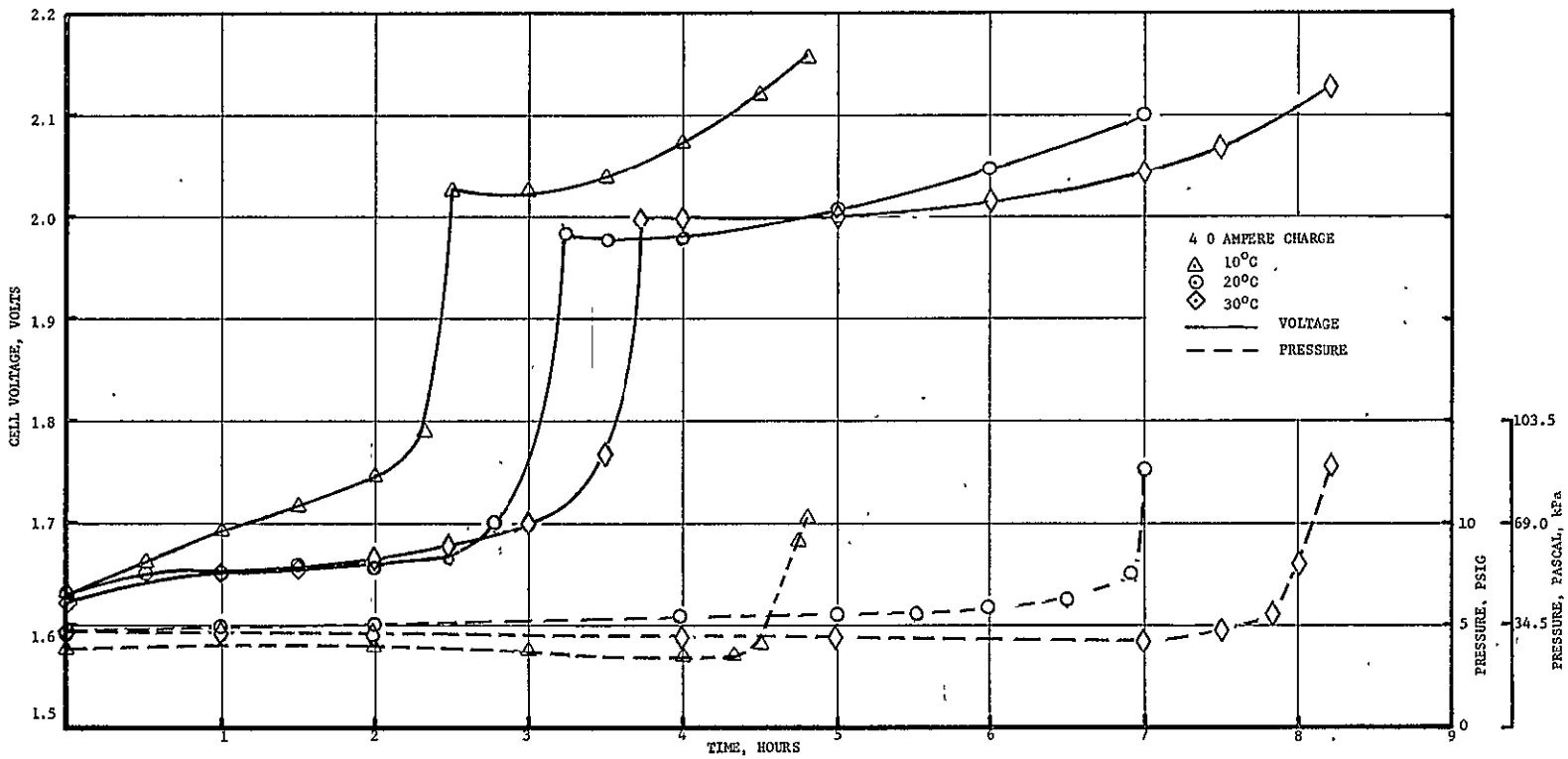


FIGURE 55 VOLTAGE PROFILE AT CYCLE NO. 1, GROUP II

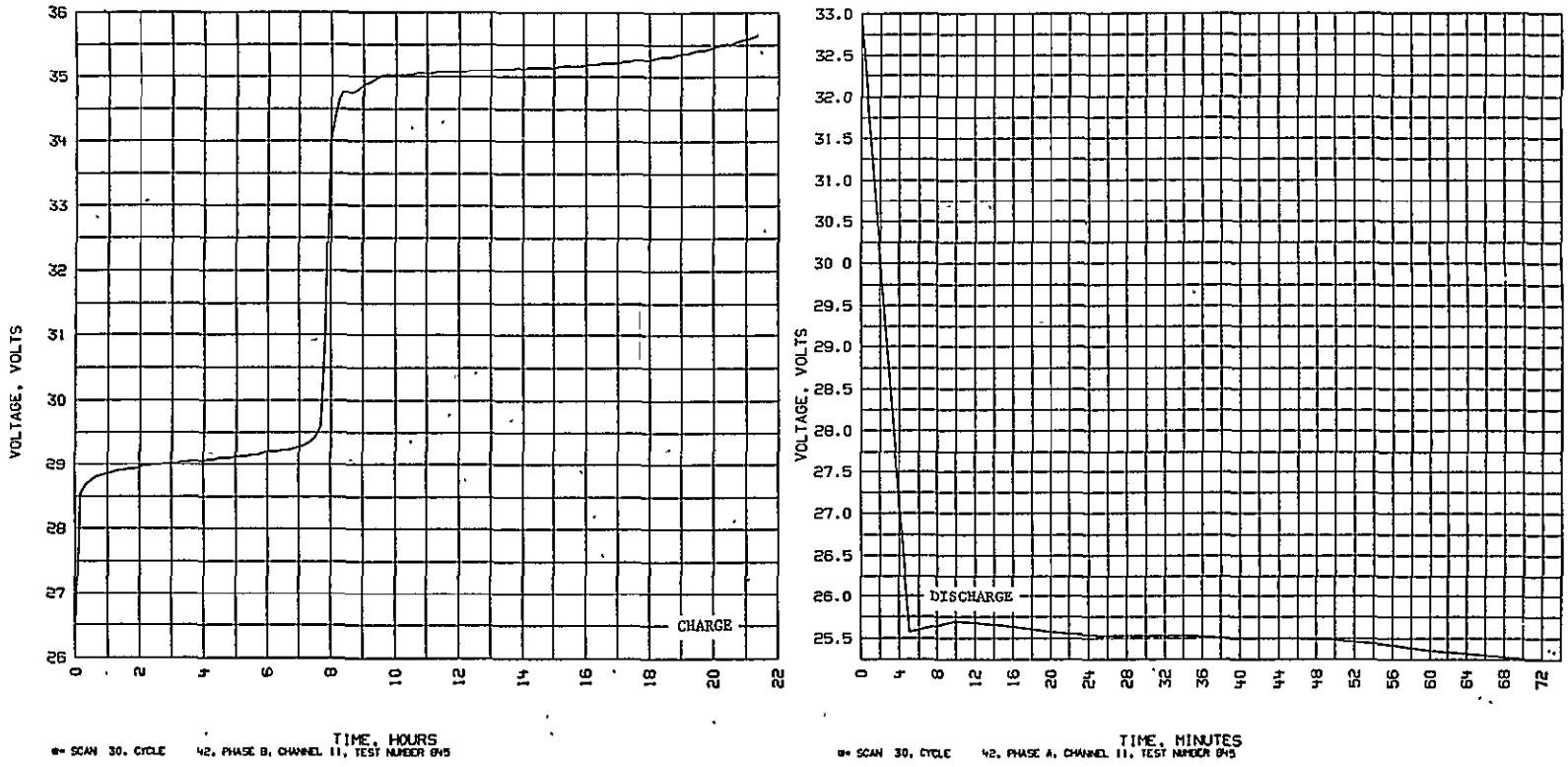


FIGURE 56 VOLTAGE PROFILE AT CYCLE NO. 42, GROUP II

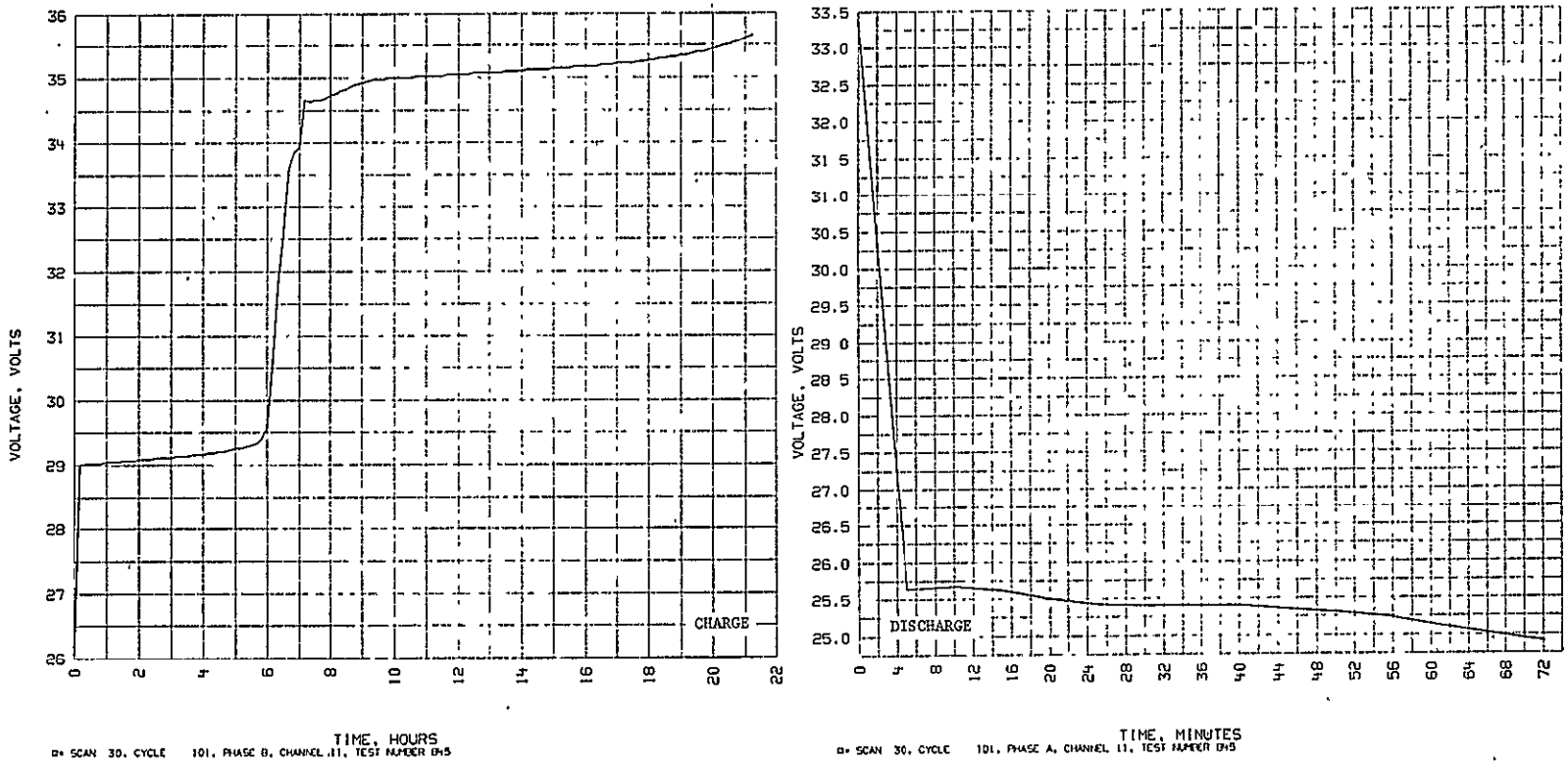


FIGURE 57 VOLTAGE PROFILE AT CYCLE NO. 101, GROUP II

FIGURE 58 INTERNAL CELL PRESSURE FOR CELLS S/N 4-138 AS A FUNCTION OF CYCLE LIFE

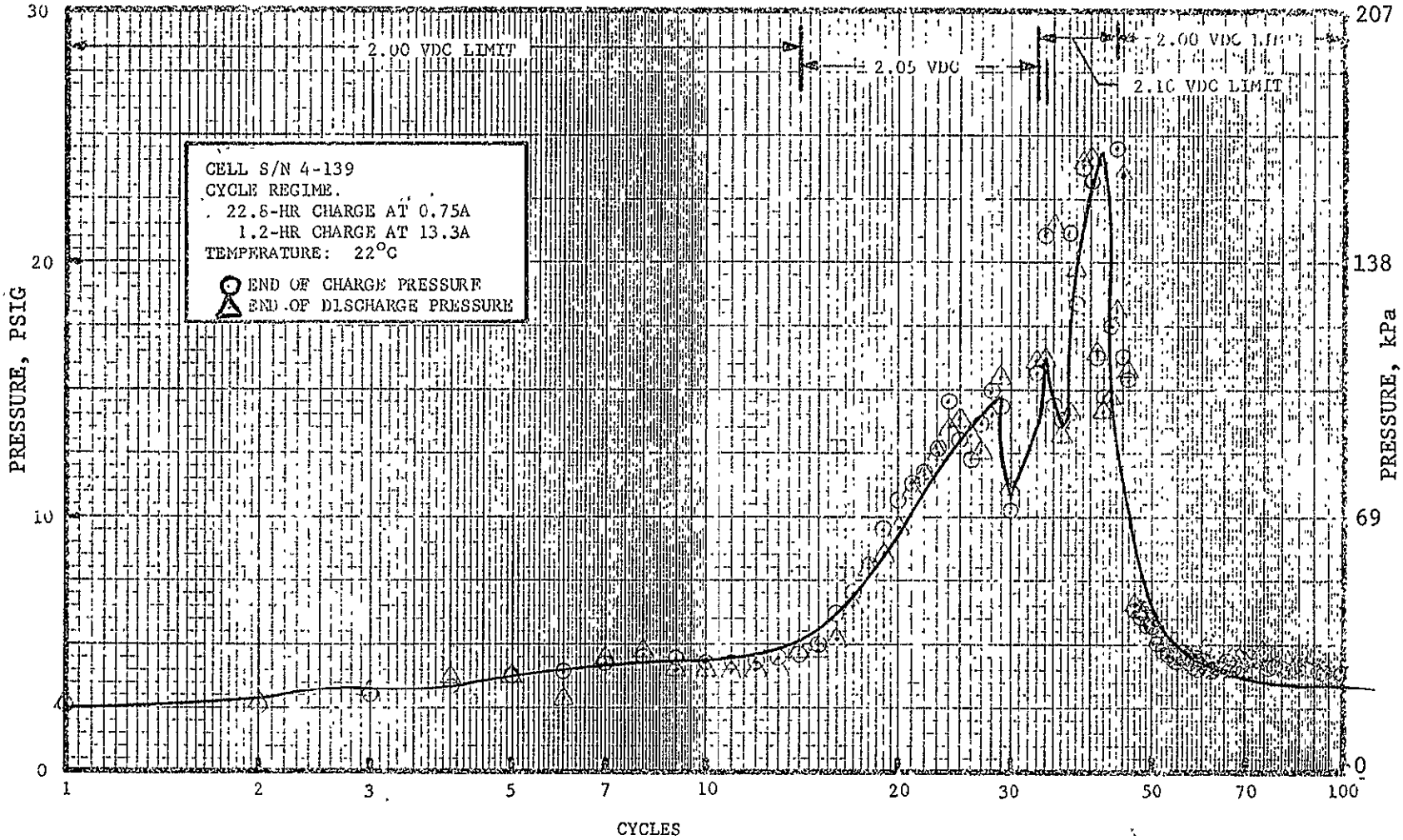


FIGURE 59 INTERNAL CELL PRESSURE FOR CELL S/N 4-139 AS A FUNCTION OF CYCLE LIFE

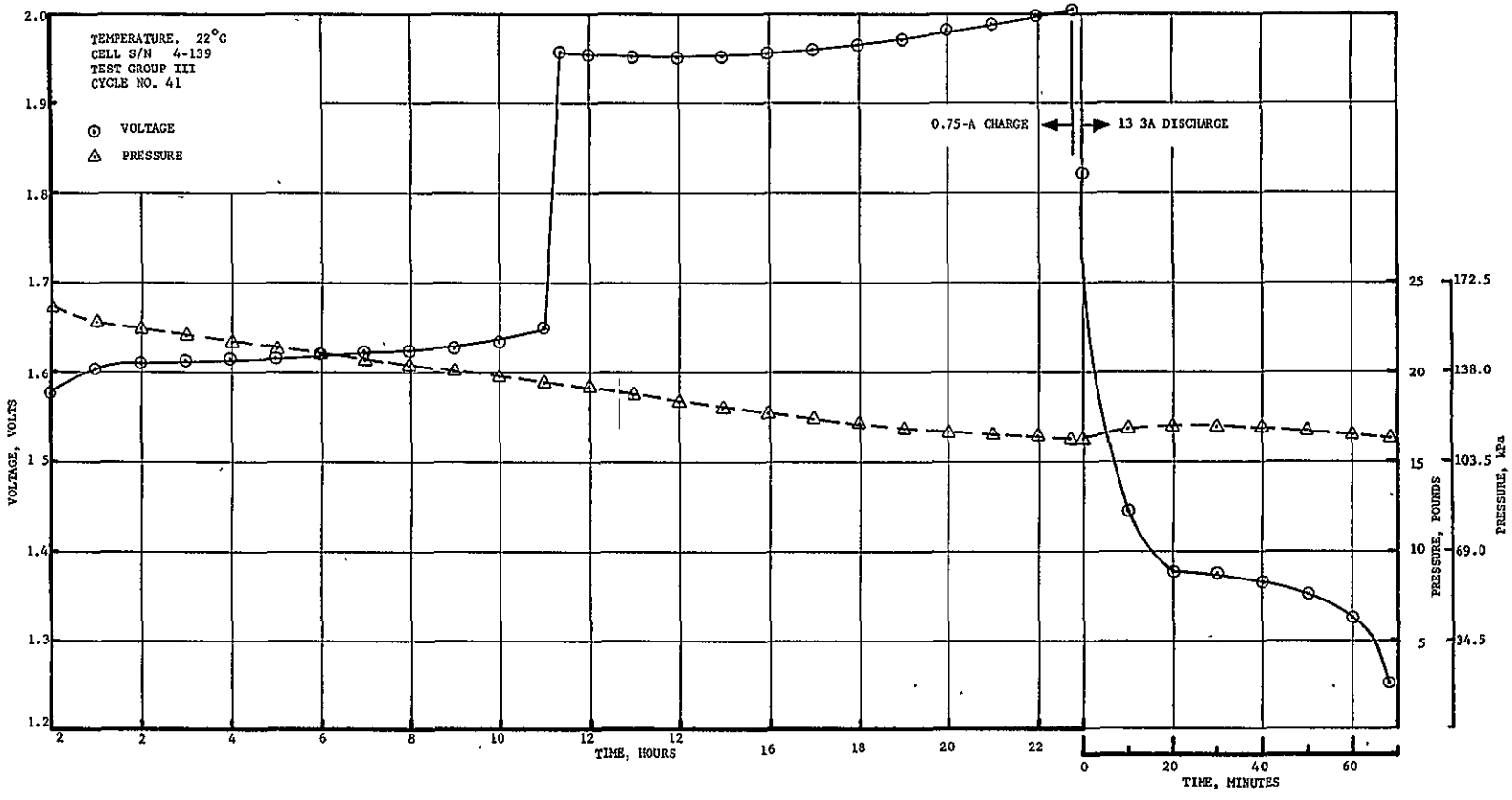


FIGURE 60 VOLTAGE/PRESSURE PROFILE AT CYCLE 41

3.5.5 Comparison of Cell-Level (Group I) vs Battery-Level (Group II) Protection

Table 9 lists the key parameters that can be compared to evaluate the possible performance differences between Group I and Group II batteries based on 100 cycles of testing. During this Phase I test period, no major differences are noticeable. However, it is significant that the cells in both battery packs are apparently well matched. In the case of battery level control, performance mismatch among the cells in one of the major failure modes. There are yet no indications of sever cell voltage divergence on the Group II battery that will lead to battery failure.

TABLE 9 COMPARISON OF GROUPS I AND II BATTERY PERFORMANCE DURING PHASE I TESTING

PARAMETERS*	GROUP I	GROUP II
Cell end of discharge voltage	1.395 Vdc	1.383 Vdc
Maximum cell EODV dispersion	54 mV	35 mV
EODV decay rate (20 to 100 cycles)	-4.1×10^{-4} V/cycle	-3.8×10^{-4} V/cycle
Cell end of charge voltage (EOCV), average	1.98 Vdc	1.98 Vdc
Maximum cell EOCV dispersion	14 mV	40 mV

*At 100th cycle, except as noted.

The other significant results of the Phase I test program are (1) the SCPs are properly terminating the charge in each cycle, (2) the SCPs do provide a more positive voltage control at the cell level, (3) both battery packs have achieved an equivalent of at least 1 year of synchronous-orbit operation.

4.0 TASK III - EVALUATION OF COMPUTER CONTROL APPROACH

4.1 TASK OBJECTIVES

The basic objective was to evaluate computer control as an alternative approach to the SCP in Task I. The scope of work was defined by NASA LeRC as follows: "Conceptual design and analysis of micro and/or mini computer approaches to single cell protection of a silver-zinc battery shall be conducted by the contractor. This work shall be performed to a degree that will permit an evaluation and comparison with the approach taken in Task II. This study shall produce comparative data on costs, performance reliability, weight, size, power consumption, and control flexibility. Based on the foregoing, a recommendation shall be made of the best approach to single cell protection for silver-zinc batteries."

4.2 APPROACH

The conceptual design was based on a microprocessor-controlled system. Known as Flexible Charge Discharge Controller (FCDC), the system was developed by Martin Marietta under an independent research and development task in 1974 and 1975. The FCDC development system is described in detail in reference 1 and was designed specifically for control and protection of nickel-cadmium batteries. Modifications of the FCDC system required to adapt it for use in Task III with silver-zinc cells consisted primarily of software changes. Hardware modifications were limited solely to minor scaling changes in the analog circuitry, which adapt the system to higher voltages characteristic of silver-zinc cells. The overall approach also included a demonstration using the Intel 8008 microcomputer on a 10-cell battery pack.

Because the cycling test is to be continued during Phase II, and the results obtained to date are inconclusive, only a partial discussion of the best approach to single cell protection for silver-zinc batteries is presented.

4.3 CONCEPTUAL DESIGN OF MICROCOMPUTER APPROACH

Essential features of the computer-based cell protector (CCP) design are illustrated in figure 61. Individual cells in the battery pack are connected in a series-wired battery configuration through a cell interconnection network. Individual cell voltages are also connected to a multiplexer where they are selected, one at a time, for monitoring. Both the multiplexer and cell interconnection network are controlled by a microcomputer via the computer interface circuitry. The microcomputer also interfaces with external input/output equipment.

[1] Imamura, M.S., et al: *Microprocessor Controlled Battery System*, paper presented at 1975 Intersociety Energy Conversion Engineering Conference.

A fundamental difference between the CCP and SCP designs is that the SCP is a "modular" approach, while the CCP is an "integrated" approach. A potential advantage of the integrated CCP approach is size reduction. Many functions that are repeated for each cell in the SCP design are reduced to a single circuit in the CCP design.

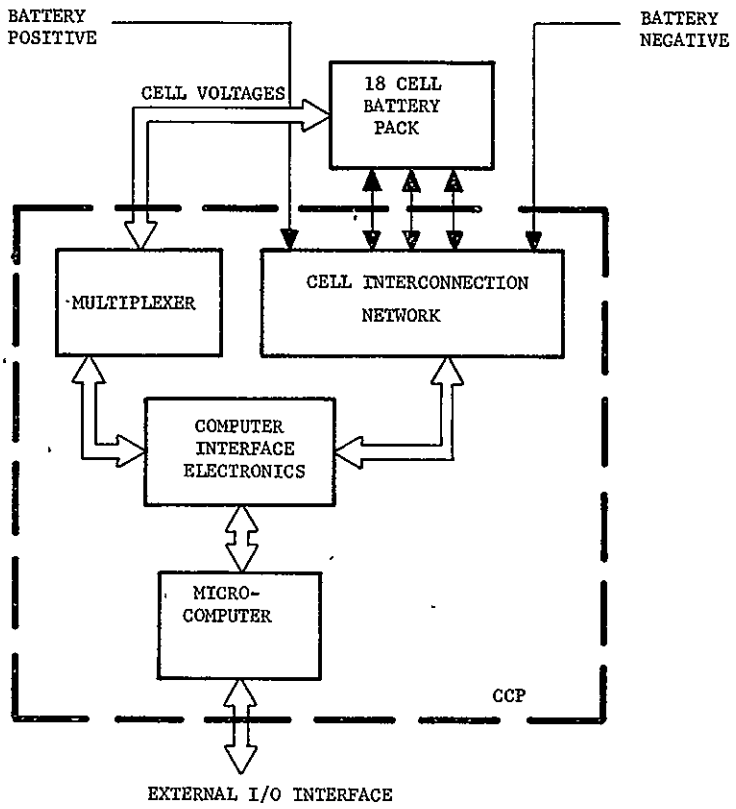


FIGURE 61 CCP BLOCK DIAGRAM

The availability of the microcomputer in the CCP design affords a potential cell control flexibility not matched by the SCP. Use of a microcomputer makes it feasible to incorporate sophisticated monitoring and control functions that would be prohibitively bulky and expensive in the modularized SCP approach. A further advantage of a microcomputer-based system is the flexibility to make last-minute design changes by reprogramming software. Hardware modifications, with their attendant effects on procurement and packaging, are eliminated. The importance of this design modification flexibility should not be underestimated. There are few applications that cannot benefit from refinement of system parameters established in the initial design phase.

4.3.1 CCP Design Considerations - The primary design requirement for the CCP was to obtain performance characteristics equal to or surpassing those of the SCP developed under Task I. A major objective of the development was to define a system with cost, performance, and reliability data established for the silver-zinc cell application. The following specific baseline design criteria were established:

1) Design a system capable of individual cell monitoring and control for up to 18 silver-zinc cells;

2) The system shall be capable of protecting the silver-zinc cells in a cycling regime as specified for Task II (i.e., 0.74-A charge rate, for 22.8 hours followed by a 13.3-A discharge for 1.2 hours);

3) The criteria for switching a cell out of circuit shall be based on cell voltage limits--provision shall be made to accommodate the voltage spike characteristic of silver-zinc cells without premature charge termination;

4) Accuracy of the cell voltage measurements shall be better than ±10 mV;

5) The system shall be capable of monitoring individual cell voltages, battery current, and individual cell status (in-circuit or out-of-circuit) via a teletype interface;

6) The system shall minimize cost, weight, power consumption, and number of piece parts.

4.3.2 CCP Description - The 18-cell CCP development system is shown in figure 62. It consists of the microcomputer, command decoder, relay drivers, relay interconnection network, multiplexer, current switch network, clock, and ancillary signal-conditioning circuits.

The cells are interconnected in series by a relay network. One relay is required for each cell. Battery connection to the charger and load bus is also made in the relay network. Magnetic latching relays, which are energized by a 50-ms pulse, are used to reduce power consumption. Relay contact position is controlled by a microcomputer. Commands to switch relays are issued by the microcomputer in the form of 8-bit binary words and are decoded by the command decoder circuit. Because of the many relays required for the CCP, reduction of the circuitry required by the relay drivers was emphasized. The number of drivers required was considerably reduced by an X-Y address arrangement whereby a given relay coil is energized when two drivers, corresponding to an X-address and Y-address, are activated.

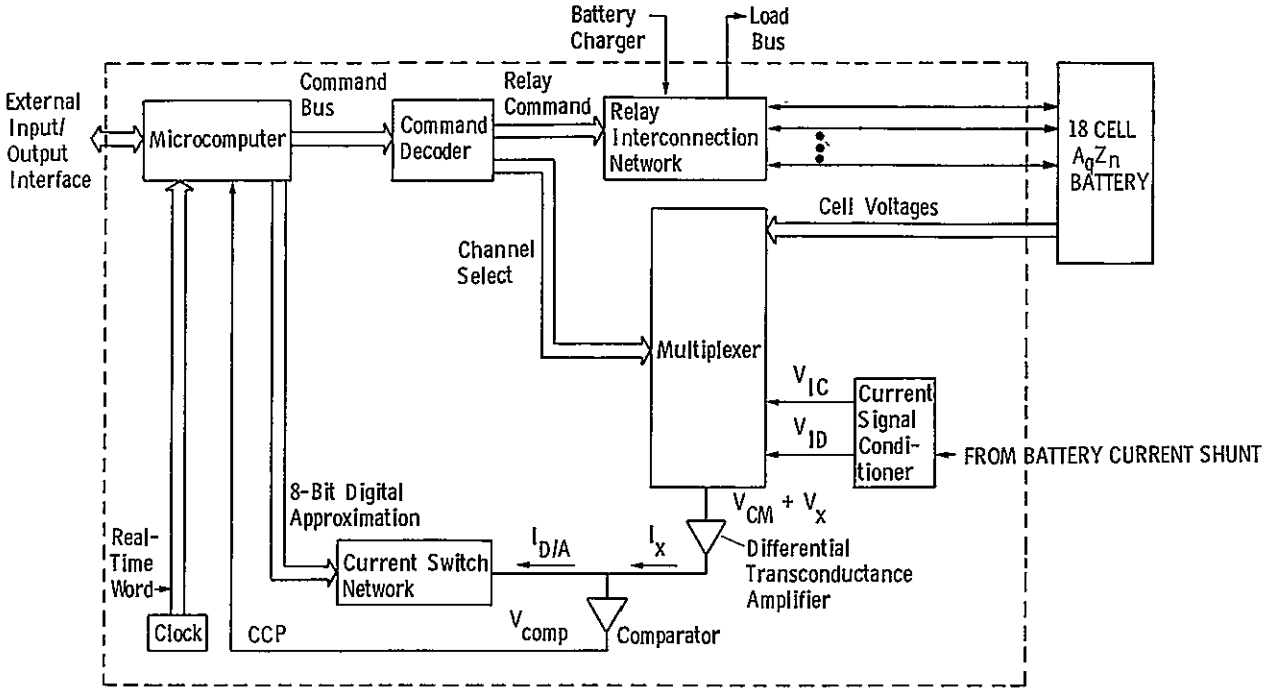


FIGURE 62. DETAILED CCP BLOCK DIAGRAM

In addition to the cell control function, the CCP also performs a monitoring function. System parameters monitored are individual cell voltages, battery current, and battery temperature. Any one of these parameters can be measured at any time. The specific parameter to be measured is selected by a multiplexer. Commands to select multiplexer channels for monitoring are issued by the microcomputer (as for the relay commands) in the form of 8-bit binary words.

The output of the multiplexer is a differential voltage, V_X, proportional to the signal being measured. The cell signal voltages are superimposed on a common mode voltage, V_{CM}, the magnitude of which depends on the position of the individual cell in the battery. This common mode voltage component is removed from the signal by a differential transconductance amplifier (DTA in figure 62) that converts the total input voltage to a current, I_X, proportional to V_X, the desired signal.

The analog signal current, I_X, proportional to the signal V_X, is converted to digital format for processing by the microcomputer. CCP parts count and power consumption are significantly reduced by using the microcomputer as an integral part of the analog-to-digital conversion. With this unique technique, the digital circuitry of conventional analog-to-digital converters is replaced by software routines. The microcomputer interfaces directly with a current switching network to generate a current, $I_{D/A}$, as an approximation of the signal current, I_X. A comparator senses

the relative magnitudes of I_X and $I_{D/A}$. The microcomputer then uses the comparator output to improve the approximation.

The development system also contains a clock that generates a real-time word. Provision for time indication permits the microcomputer to numerically integrate the battery charge and discharge ampere-hour integrals. The ampere-hour integrals can be used to implement charge control techniques that use recharge fraction (ratio of ampere-hours in to ampere-hours out), in addition to cell voltage, for terminating battery charging.

The microcomputer is the central element around which the CCP is constructed. It controls battery cell interconnection as well as acquisition and interpretation of data on critical battery parameters. In addition, it provides the interface with remote ground or flight data handling systems.

The addition of circuitry to condition battery current and temperature for signal processing completes the CCP system.

Battery Interface - The battery interconnection network is shown in figure 63. An individual magnetic latching relay is provided for each

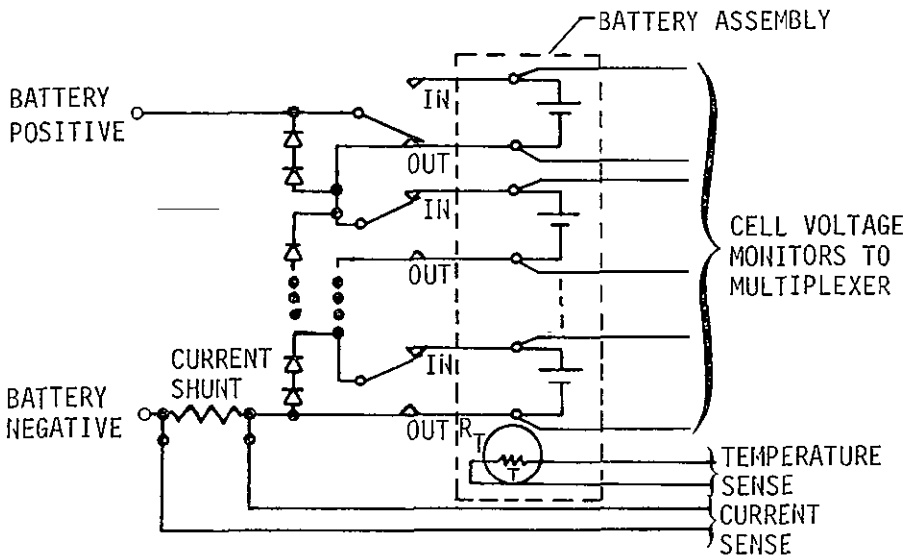


FIGURE 63 BATTERY/CCP INTERFACES

cell and wired so that the cell can be switched into or out of a series connection by command. Voltage monitor leads from the multiplexer are also connected directly to each cell terminal for monitoring. Direct connection to the cell terminals, rather than to the relay terminals, eliminates measurement errors caused by current flow through the interconnecting wiring and relay contact resistance.

Cell by-pass diodes are connected to each relay in an "alternative path" arrangement. These diodes are not necessary for fundamental control of cell switching, but may be desired in a specific application because:

1) The diodes provide an alternative path for battery discharge current flow during relay contact switching transitions--they thus prevent the load bus from being open-circuited from the battery during relay contact transition time;

2) By virtue of their current shunting action, the diodes provide suppression for the relay contacts. If a relay is commanded to switch a cell out of the battery group under conditions of heavy discharge, the voltage through which the current must be switched is clamped to the small forward drop of the diodes.

Relay Driver Circuit - Commitment of an individual relay to each cell in the battery implies extensive circuitry for relay coil drivers. Two coils on each relay impose a requirement to drive 36 relay coils for the 18-cell battery network. The circuitry required for individual relay drivers would have a significant impact on overall CCP size.

To reduce the parts count in the relay driver circuit, an X-Y addressing scheme was selected for the development system, as shown in figure 64. This arrangement requires two drivers, corresponding to both an

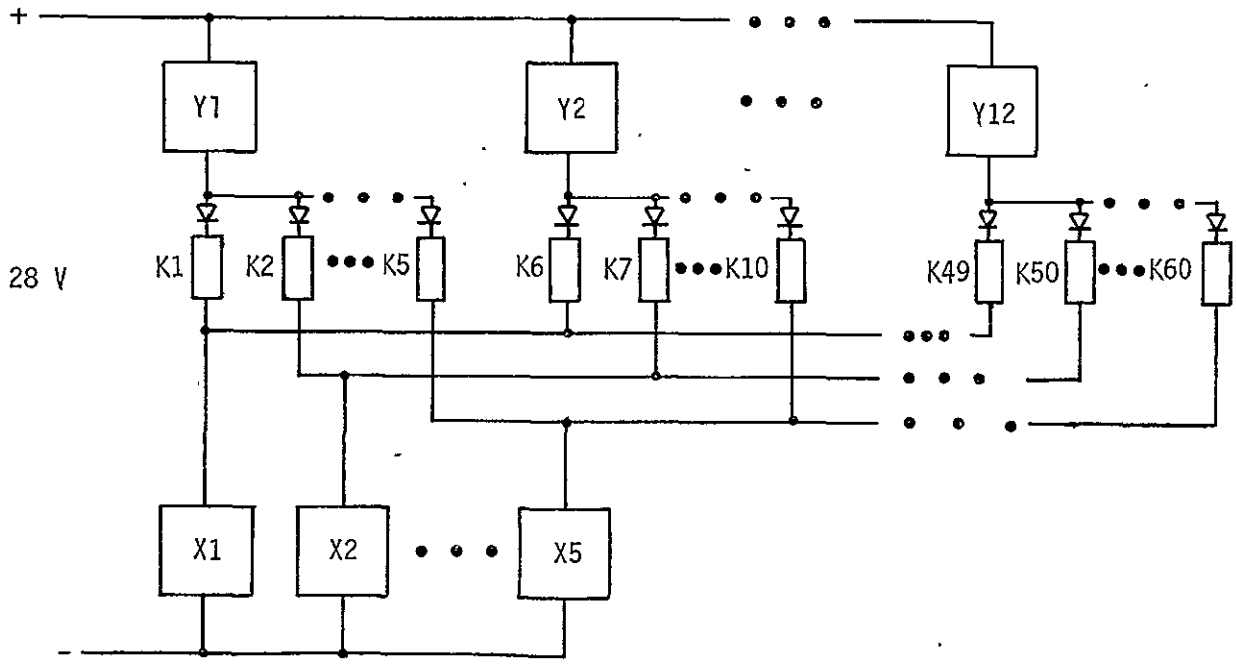


FIGURE 64 RELAY DRIVER NETWORK

X- and a Y-address, to be activated to energize a given relay coil. The X drivers are arranged to provide "negative leg" switching for the coils, the Y drivers to provide "positive leg" switching. To energize coil K6 (figure 4.3-4), for example, drivers Y2 and X1 must both be operating. The circuit of figure 4.3-4 requires 11 driver circuits to control 36 relay coils, resulting in a reduction in parts count by a factor greater than 3 over mechanization with individual drivers for each coil. However, steering diodes are required in series with each relay coil to prevent current flow through "sneak paths" that are created when multiple coils are tied to a common point.

Command Decoder - The command decoder circuit provides compatible interface between the microcomputer and the rest of the CCP electronics, and converts the binary coded microcomputer command words to command signals for direct control of monitoring and relay switching circuits.

The command decoder circuit is shown in figure 65. Decoder circuitry is divided into two sections, corresponding to two different bias

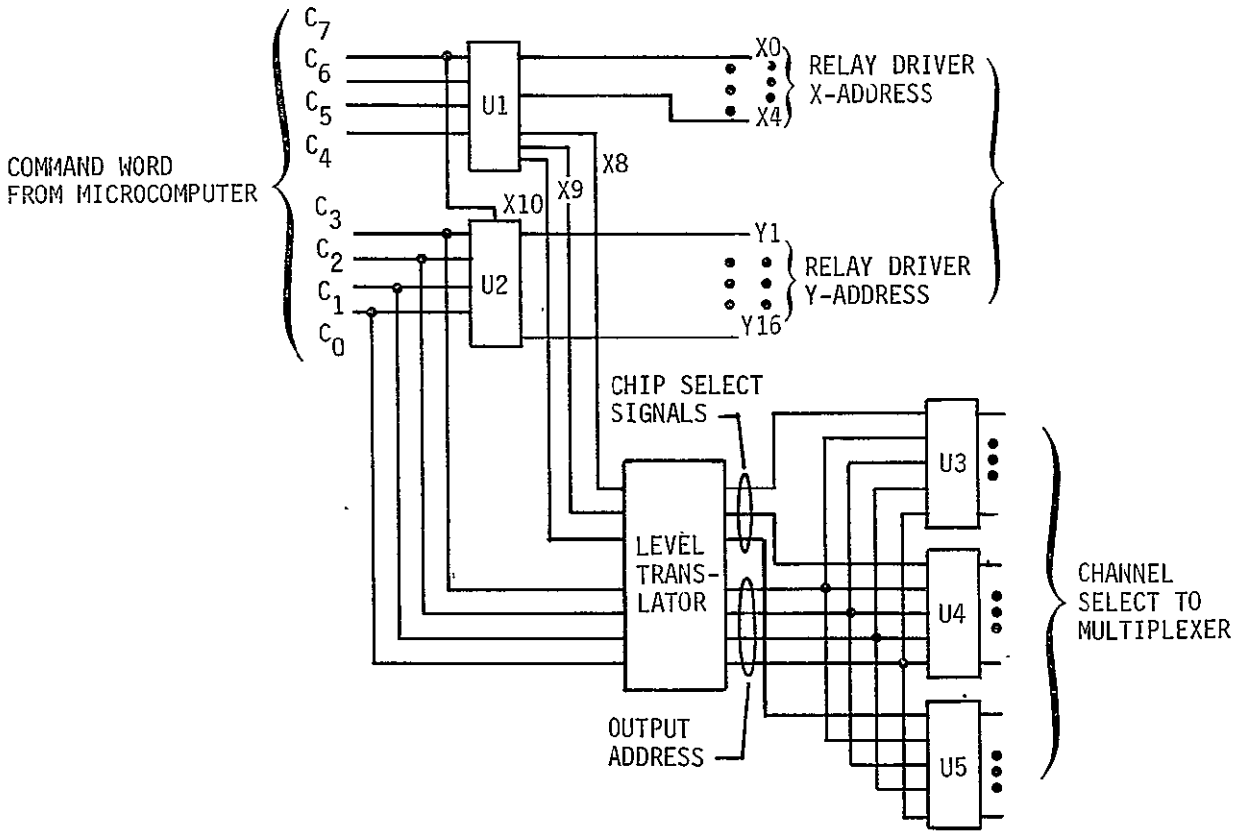


FIGURE 65 COMMAND DECODER

levels. The first section, consisting of U1 and U2, is biased between ±5 V and ground. Decoded signals from this section are used to provide the X- and Y-addresses for the relay drivers and three multiplexer channel group select signals (X8, X9, X10). Each decoder element (U1 or U2) operates on four bits of the command word, converting them to a selected 1 of 16 output. The upper 4 bits of the command word, $C_7C_6C_5C_4$, are decoded by U1, the lower 4 bits, $C_3C_2C_1C_0$, by U2.

The second section of the decoder circuitry provides multiplexer channel select signals. This section is biased between -5 and -10 V for compatibility with the multiplexer drivers. Voltage level translation is provided for the four least significant bits of the command word, $C_3C_2C_1C_0$, and three decoded signals (X8, X9, X10) from the $C_7C_6C_5C_4$ decoder section. The three decoded signals, X8, X9, and X10, are used to select one of three 16-line decoder elements, U3, U4, or U5. The actual decoder output addressed is then determined by the 4-bit command word, $C_3C_2C_1C_0$.

Multiplexer - Like the relay drivers, the multiplexer is a circuit in which parts count reduction is of primary importance. Each cell in the battery requires an associated multiplexer channel, and the need to reduce voltage errors in the interconnecting wire and relay contacts prevents circuit reduction by allowing one multiplexer input to serve as both the positive terminal sense point for one cell and the negative terminal sense point for an adjacent cell. To compound the problem, commercially available integrated circuit multiplexers are incapable of handling the high common-mode voltages required for a battery interface. In addition, the power consumption of integrated circuit multiplexers becomes a significant drawback to their use in a CCP system projected for spacecraft applications.

The unavailability of integrated-circuit multiplexers forces design of a discrete circuit, a schematic of which is shown in figure 66. This circuit requires three parts per switch, or six parts for each multiplexer channel. The three parts of each switch are the contact (QA and QC in figure 66), a bleed resistor for proper field effect transistor (FET) biasing (R), and a driver (QB and QD). To reduce weight and volume, this circuit can be hybridized with several multiplexer channels in one hybrid package.

The input impedance of a single multiplexer input in the "off" state is approximately the impedance of the bleed resistor, 1 MΩ. In the "on" state, the input impedance is even higher, many megohms, because while the switch is on, it connects the signal to a high-impedance operational amplifier circuit that draws negligible circuit.

FETs were selected for the switch drivers for two reasons: (1) a single FET will interface with a CMOS integrated circuit decoder without additional biasing circuitry; (2) if the multiplexer is connected to a battery without the CCP powered up, the FET drivers will be "on" holding the

FET contacts "off." Because of multiple switches operating simultaneously, random interconnection of signals is thereby avoided.

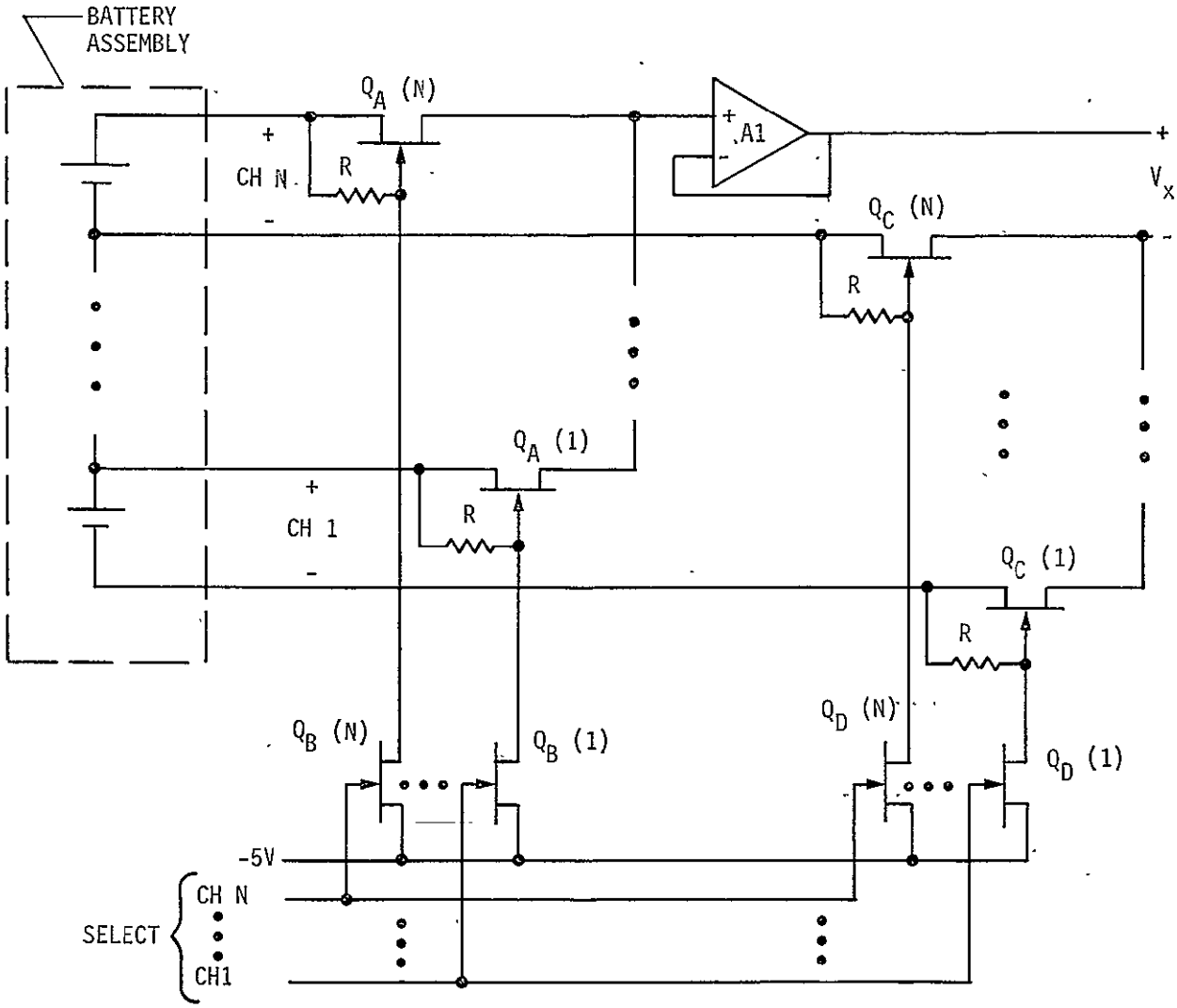


FIGURE 66 MULTIPLEXER

Differential Transconductance Amplifier - The accurate measurement of a small signal voltage (e.g., a cell voltage) superimposed on a large common-mode voltage (e.g., a battery) is a difficult circuit design problem.

A conventional method of obtaining this measurement is to use a differential amplifier circuit configuration as was done in the SSVC design. However, the differential amplifier is severely handicapped by error sensitivity coefficients for the four feedback resistors in the differential amplifier that produce an error in the output voltage that is amplified out of proportion to the resistor error source. This error amplification effect is caused by the presence of the common mode voltage. The common-mode voltage problem is described in detail in relation to the SSVC design in section 2.4.

To avoid these high resistor sensitivity factors, two design approaches are open. First, the gain of the differential amplifier can be increased, resulting in a decrease in the sensitivity factors. This approach also increases the common mode input to the operational amplifier, and precludes the use of commonly available integrated-circuit operational amplifier for the CCP application where common mode voltages to 40 Vdc are possible. A second approach is to change the circuit configuration to a type that has inherently low sensitivity factors. The second approach was chosen for both the SCP and CCP designs. In the SCP design, an isolation regulator was developed that provided a floating reference for circuit operation. In effect, the SCP monitor circuits sensed the cell voltage without a common mode component.

The CCP approach relies on the development of a differential transconductance amplifier shown in figure 67. The input voltage signal, V_x,

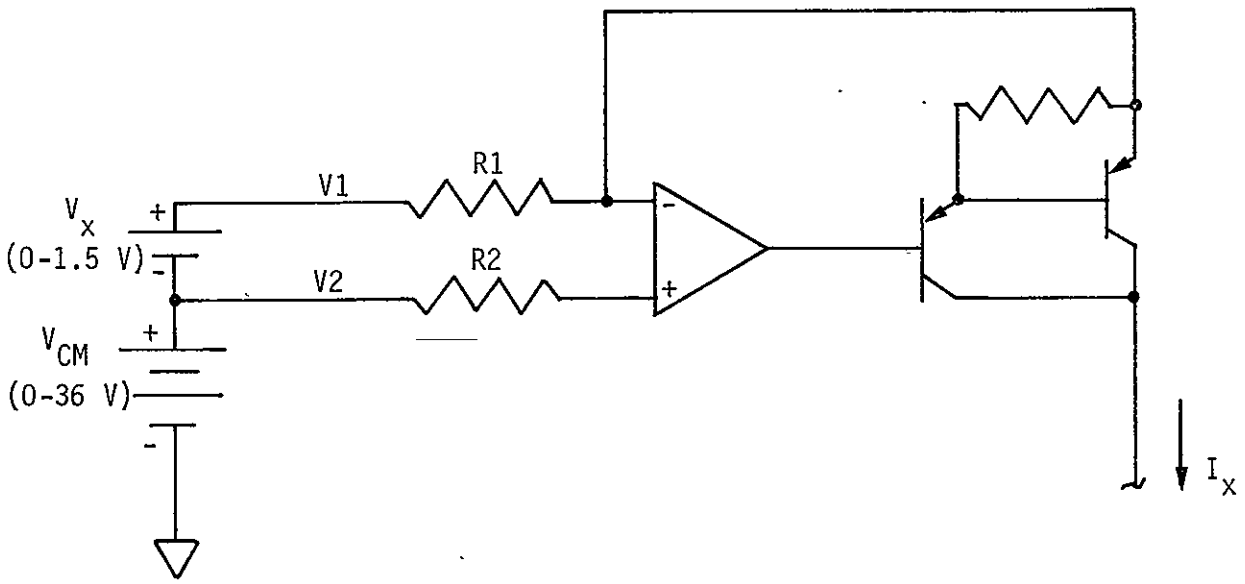


FIGURE 67. DIFFERENTIAL TRANSCONDUCTANCE AMPLIFIER

is converted to a current signal, I_x, according to the relation

$$I_x = \frac{V1 - V2}{R1} = \frac{V_x}{R1} .$$

The differential transconductance amplifier configuration is inherently insensitive to common mode voltage. No stringent resistor matching requirements are imposed, and indeed, the significant error sources are reduced from four to one: the resistor R1. The sensitivity factor of R1 itself is

independent of the common mode voltage, a 1.0% change in R1 producing a 1.0% change in the output that is independent of the common mode voltage.

Analog-to-Digital Conversion - The availability of a microcomputer in the CCP permits significant reduction in analog-to-digital conversion circuitry by replacing digital hardware found in conventional analog-to-digital converters with software routines. The analog current output, I_x, of the differential transconductance amplifier is the parameter converted to digital format for processing by the microcomputer.

Circuitry required to implement the converter is reduced to a current switching network and an output comparator, as shown in figure 68. Two quad current switch networks--with associated bias resistors--are used to accommodate an 8-bit digital approximation word from the microcomputer. Proper current switch biasing is established by amplifier A1. The output currents, I_1 and I_2, are then summed (with I_2 properly scaled by R_1 and R_2) to form an analog signal, $I_{D/A}$, proportional to the digital approximation.

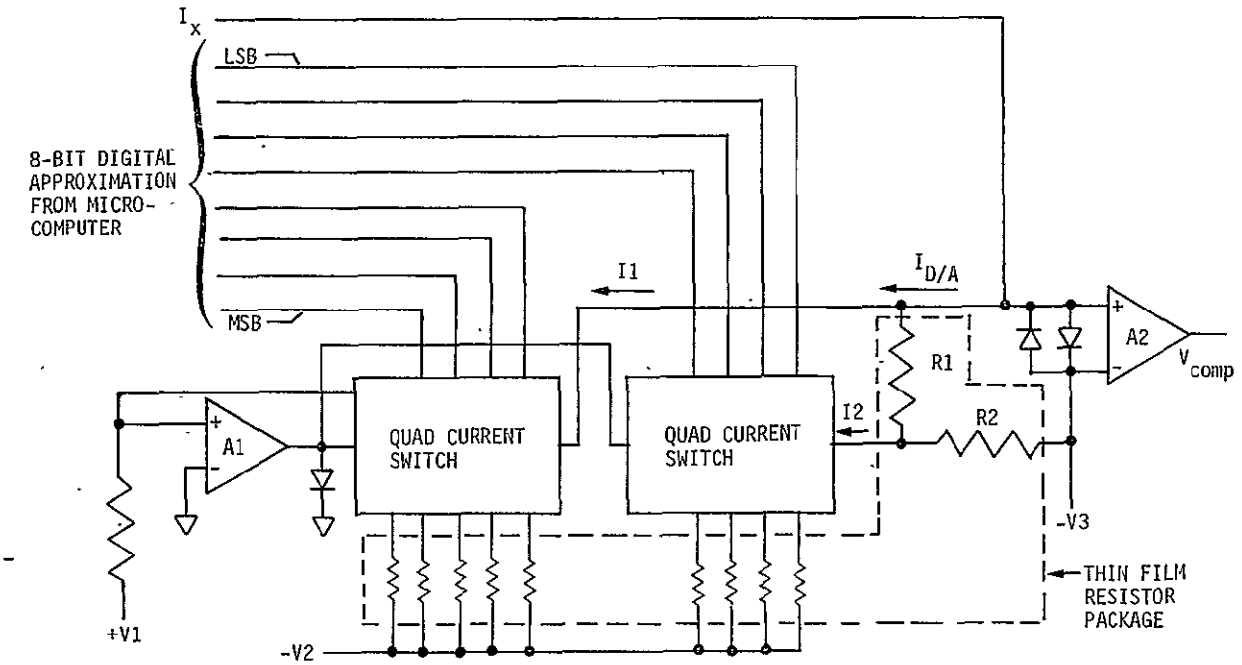


FIGURE 68 D/A CONVERTER

The relative magnitude of the input signal current, I_x, and the digital estimation current, $I_{D/A}$, is sensed by comparator A_2. If I_x is greater than $I_{D/A}$, the comparator output is high. If I_x is less than $I_{D/A}$, the comparator output is low.

In a typical analog-to-digital conversion cycle, the microcomputer will first issue an 8-bit approximation word with only the most significant bit true. The resultant $I_{D/A}$ current will then be half of full scale in magnitude. If I_x exceeds $I_{D/A}$, the comparator output is high, and this information is used by the microcomputer to improve the approximation. The next approximation word issued will retain the most significant bit true and will contain the second most significant bit true. If I_x is less than $I_{D/A}$, the second approximation word issued will have the most significant bit reset to false, and only the second most significant bit set true. Eight approximation cycles are required to complete an analog-to-digital conversion, one cycle for each bit in the digital approximation word. At the completion of the eight cycles, an accurate 8-bit digital representation of the signal current, I_x, is stored in the microcomputer.

Although the microprocessor is an 8-bit machine, the analog-to-digital conversion accuracy is not limited to 8 bits. Addition of a third quad current switch network and another microcomputer output port permits extension of the converter accuracy to 12 bits. Implementation of a 12-bit converter (or of any converter between 9- and 16-bit accuracy) would require the microcomputer to operate on digital information in a double precision mode.

For CCP application, 8 bits were considered sufficiently accurate to meet circuit performance objectives. A digital resolution error of ±0.2% is obtained, which, for a silver-zinc cell with a full-scale voltage of 2.15, corresponds to an error of ±4.2 mV.

The analog-to-digital conversion routine implemented in the CCP requires 4 ms to complete a conversion. The time required to monitor all system paramenters (30 individual cell voltages, battery current, and battery temperature) is less than 150 ms. While this conversion speed is rather slow compared to the capabilities of today's high-speed converters, it is more than adequate for the CCP application.

Clock - The clock is implemented with a 524-kHz oscillator and countdown circuit. The oscillator is shared with the microcomputer. The countdown circuit consists of two 14-stage CMOS ripple counters. The clock output is a 6-bit binary word, representing real time, which is fed back to the microcomputer. Time data are used by the microcomputer to perform ampere-hour integration.

Ampere-hour integration is obtained by a software routine that multiplies battery current by a time interval to obtain an increment of charge. Each increment of charge thus calculated is added to a sum that represents accumulated charge, i.e., the ampere-hour integral. The time increment used in the numerical integration calculation is 1 s and corresponds to the least significant bit of the clock real-time word. In normal operation when the CCP is cycling continuously through the monitor routine, the real-

time word is interrogated several times per second. Whenever a change in the real-time word is detected, the charge increment is calculated and the ampere-hour integration updated. Under abnormal conditions-when the CCP is servicing external commands, for example, it may not be possible for the microcomputer to query the real-time word every second. To avoid loss of charge integrating capability under these conditions, the elapsed time for which the microcomputer is busy is accumulated by the real-time word, and, when the microcomputer returns to the ampere-hour routine, the elapsed time is used as the time interval in the charge increment calculation. With the 6-bit real-time word, the microcomputer can be diverted for up to 64 s without missing an increment in the integration.

Microcomputer - The microcomputer is the heart of the CCP. Figure 69 is a simplified diagram of the CCP microcomputer using the Intel 8080 microprocessor as the central processing unit (CPU). The memory is

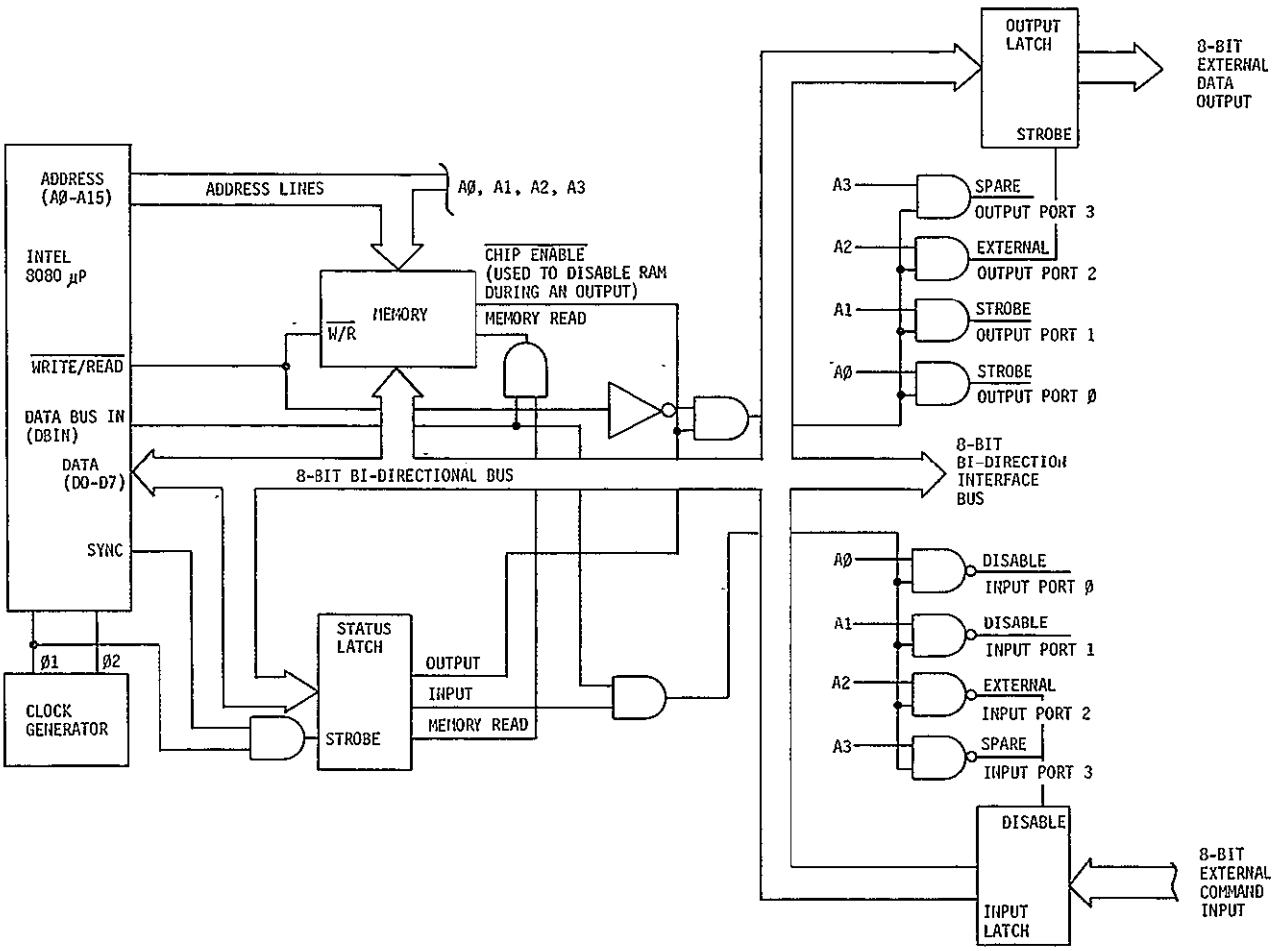


FIGURE 69 CCP MICROCOMPUTER USING INTEL 8080 MICROPROCESSOR

a combination of low-power read-only memory (ROM) for program storage and random-access memory (RAM) for variable parameter and data storage. The memory chips were selected mainly for low power consumption. The interface between the microcomputer and other CCP electronics is via a common 8-bit bidirectional data bus. Discrete signals used for entering data from and to the computer on the data bus are furnished by the CPU. Further input and output expansion is provided by spare discretes. Two 8-bit latches with a 3-state output are used for interfacing with a ground or spacecraft data handling system. The status latch is used by the CPU for controlling data flow in the microcomputer. The microcomputer system shown in figure 69 uses 8 ICs plus memory and oscillator.

We have chosen the 8080 microprocessor because of significant software advantages (78 vs 48 instructions), fewer piece parts, and direct interface capability with the low-power CMOS circuits.

4.3.3 Software Description - CCP software was developed with two primary objectives: (1) to functionally simulate essential features of the CCP (i.e., charge and discharge limit detection and cell switching, and accommodation of the silver-zinc voltage spike characteristic); (2) to exploit data acquisition capabilities inherent in the CCP design.

Command Word Structure - Key considerations for CCP software were minimum memory chips, simple starting capability, control flexibility, and monitoring.

The approach used to minimize memory requirements was to incorporate design techniques that make efficient use of memory. The structure of the basic 8-bit command word is the key to this design technique. It is common in many systems to allocate a memory location to each command. When stored in this manner, commands can be easily modified by a change in memory content rather than by reprogramming a command sequence. However, a large command list will require proportionate memory size. Therefore, the CCP development system does not use an addressable command implementation. The CCP command word is divided into two parts; a function field and an address field:

$$\underbrace{C_7C_6}_{\text{Function Field}} \qquad \underbrace{C_5C_4C_3C_2C_1C_0}_{\text{Address Field}}$$

The address field defines a given cell; the function field defines the particular operation to be performed on that cell. These operations are monitor voltage, disconnect from battery, or connect to battery. For example, the three operational commands pertaining to cell number five would be coded as follows:

10-000101, monitor cell voltage

00-000101, disconnect cell from battery

01-000101, connect cell to battery

With this CCP command word structure, a monitor routine can be performed by sequentially incrementing the address field as shown below.

Cell Monitored	Monitor Command
1	10-000001
2	10-000010
⋮	⋮
18	10-010010

(incrementing by 1)

If an out-of-limits condition is detected on a particular cell, the cell is commanded "off" by complementing the most significant bit in the present cell monitor command function field. Similarly, the command to connect a cell to the battery can be constructed from the monitor command for that cell by merely complementing the two most significant bits of the function field.

Memory Assignment - Parameters stored in memory for use in the computer program are summarized in table 10. A complete list of these parameters, their memory location, and their initial contents at the time of loading is shown in table 10.

TABLE 10 CCP PROGRAM PARAMETERS

VARIABLES	CONSTANTS
Battery current	Charge/discharge voltage limits
All cell voltages	Monoxide/peroxide transition voltage
	Inhibit time limit
All cell inhibit time delays	Charge- & discharge-mode data-dump time limit
Cell status words (4)	Start/end data dump addresses (housekeeping)
Charge/discharge cycle count	
Clock time	End of status words flag (housekeeping)
Data dump time	
Interim cell voltage storage (housekeeping)	
Word count (housekeeping)	

In addition to their use by the microcomputer in the calculation of operational commands, parameters stored in memory represent a data bank

TABLE 11 STATUS WORD FORMAT

MEMORY LOCATION (OCTAL)	CONTENTS (OCTAL)	PROGRAM USAGE	DESCRIPTION	
Ø12:124:	113	Constant	Data Dump Time, Discharge Mode (6 minutes)	
Ø12:125:	ØØØ	---	Spare	
Ø12:126:	ØØØ	Variable	Clock Time	
Ø12:127:	337	Variable	Data Dump Counter (preset to 5 seconds)	
Ø12:13Ø:	341	Constant	Data Dump Time, Charge Mode (30 minutes)	
Ø12:131:	ØØØ	Variable	Interim Cell Voltage Storage (Housekeeping)	
Ø12:132:	151	Constant	Inhibit Time Limit	
Ø12:133:	3Ø2	Constant	Monoxide/Peroxide Transition Voltage	
Ø12:134:	ØØØ	---	Spare	
Ø12:135:	345	Constant	Cell Charge Voltage Backup Limit	
Ø12:136	335		Cell Charge Voltage Limit	
Ø12:137:	173		Cell Discharge Voltage Backup Limit	
Ø12:14Ø:	214		Cell Discharge Voltage Limit	
Ø12:141:	226	Constant	End of Data Dump Address (Housekeeping	
Ø12:142:	ØØØ	Variable	Charge-Discharge Cycle Count	
Ø12:143:	ØØØ	Variable	Word Count (Housekeeping for carriage return)	
Ø12:144:	17Ø	Constant—	Start of Data Dump Address (Housekeeping)	
Ø12:145:	ØØØ	---	Spare	
Ø12:146:	ØØØ	Variable	Cell No. 1	Time Delay From Start of Monoxide/Peroxide Transition 1 LSB =
Ø12:147:	ØØØ		Cell No. 2	
Ø12:15Ø:	ØØØ		Cell No. 3	
Ø12:151:	ØØØ		Cell No. 4	
Ø12:152:	ØØØ		Cell No. 5	
Ø12:153:	ØØØ		Cell No. 6	
Ø12:154:	ØØØ		Cell No. 7	
Ø12:155	ØØØ		Cell No. 8	
Ø12:156:	ØØØ		Cell No. 9	
Ø12:157:	ØØØ		Cell No. 10	

TABLE 11 (CONTINUED)

MEMORY LOCATION (OCTAL)	CONTENTS (OCTAL)	PROGRAM USAGE	DESCRIPTION	
Ø12:160:	ØØØ	Variable	Cell No. 11	Time Delay From Start of Monoxide/Peroxide Transition 1 LSB =
Ø12:161:	ØØØ		Cell No. 12	
Ø12:162:	ØØØ		Cell No. 13	
Ø12:163:	ØØØ		Cell No. 14	
Ø12:164:	ØØØ		Cell No. 15	
Ø12:165:	ØØØ		Cell No. 16	
Ø12:166:	ØØØ		Cell No. 17	
Ø12:167:	ØØØ	Variable	Cell No. 18	
Ø12:17Ø:	ØØØ	---	Spare	
Ø12:171:	ØØØ	---		
Ø12:172:	ØØØ	---		
Ø12:173:	ØØØ	---		
Ø12:174:	ØØØ	---		
Ø12:175:	ØØØ	---		
Ø12:176:	ØØØ	---		
Ø12:177:	ØØØ	---	Spare	
Ø12:2ØØ:	ØØØ	Variable	Battery Current (1 LSB =)	PARAMETER PRINTED OUT IN DATA DUMP
Ø12:2Ø1:	ØØØ		Cell No. 1 Voltage	1 LSB =
Ø12:2Ø2:	ØØØ		Cell No. 2 Voltage	
Ø12:2Ø3:	ØØØ		Cell No. 3 Voltage	
Ø12:2Ø4:	ØØØ		Cell No. 4 Voltage	
Ø12:2Ø5:	ØØØ		Cell No. 5 Voltage	
Ø12:2Ø6:	ØØØ		Cell No. 6 Voltage	
Ø12:2Ø7:	ØØØ		Cell No. 7 Voltage	
Ø12:21Ø:	ØØØ		Cell No. 8 Voltage	
Ø12:211:	ØØØ		Cell No. 9 Voltage	
Ø12:212:	ØØØ		Cell No. 10 Voltage	
Ø12:213:	ØØØ		Cell No. 11 Voltage	
Ø12:214:	ØØØ		Cell No. 12 Voltage	
Ø12:215:	ØØØ	Variable	Cell No. 13 Voltage	

TABLE 11 (CONCLUDED)

MEMORY LOCATION (OCTAL)	CONTENTS (OCTAL)	PROGRAM USAGE	DESCRIPTION
Ø12:216:	ØØØ	Variable	Cell No. 14 Voltage } 1 LSB = PARAMETER PRINTED OUT IN DATA DUMP
Ø12:217:	ØØØ		Cell No. 15 Voltage
Ø12:22Ø:	ØØØ		Cell No. 16 Voltage
Ø12:221:	ØØØ		Cell No. 17 Voltage
Ø12:222:	ØØØ		Cell No. 18 Voltage
Ø12:223:	ØØØ		Status Word No. 1
Ø12:224:	ØØØ		Status Word No. 2
Ø12:225:	ØØØ		Status Word No. 3
Ø12:226:	ØØØ		Status Word No. 4
Ø12:227:	ØØØ	Constant	End of Status Words Flag (Housekeeping)

STATUS WORD	NO. 1			NO. 2			NO. 3			NO. 4		
OCTAL CODE	W_2	W_1	W_0	W_2	W_1	W_0	W_2	W_1	W_0	W_2	W_1	W_0
BINARY CODE	0 0	0 0 0	0 0 0	0 0	0 0 0	0 0 0	0 0	0 0 0	0 0 0	0 0	0 0 0	0 0 0

.ESCRIPTION

SPARE

1 1 1 1 1 1 1 1 1

8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 SPARE

CELL STATUS

0 = CELL IN CIRCUIT

1 = CELL OUT OF CIRCUIT

MODE: 0 = DISCHARGE

1 = CHARGE

of useful information on which to periodically draw and "dump" to an external output device (magnetic tape, disk, or teletype) for logging and reduction. Data selected for dumping are battery current, cell voltages, and the four cell status words. The cell status words identify which cells are in-circuit, which are out-of-circuit, and whether the battery is in the charge or discharge mode. A sample of teletype printout for the CCP program is shown in figure 70.

Program Description - The basic software flow diagram for the CCP is shown in figure 71. There are three major subroutines: START, CHARGE, and DISCHARGE. The program is entered via the start routine. To proceed,

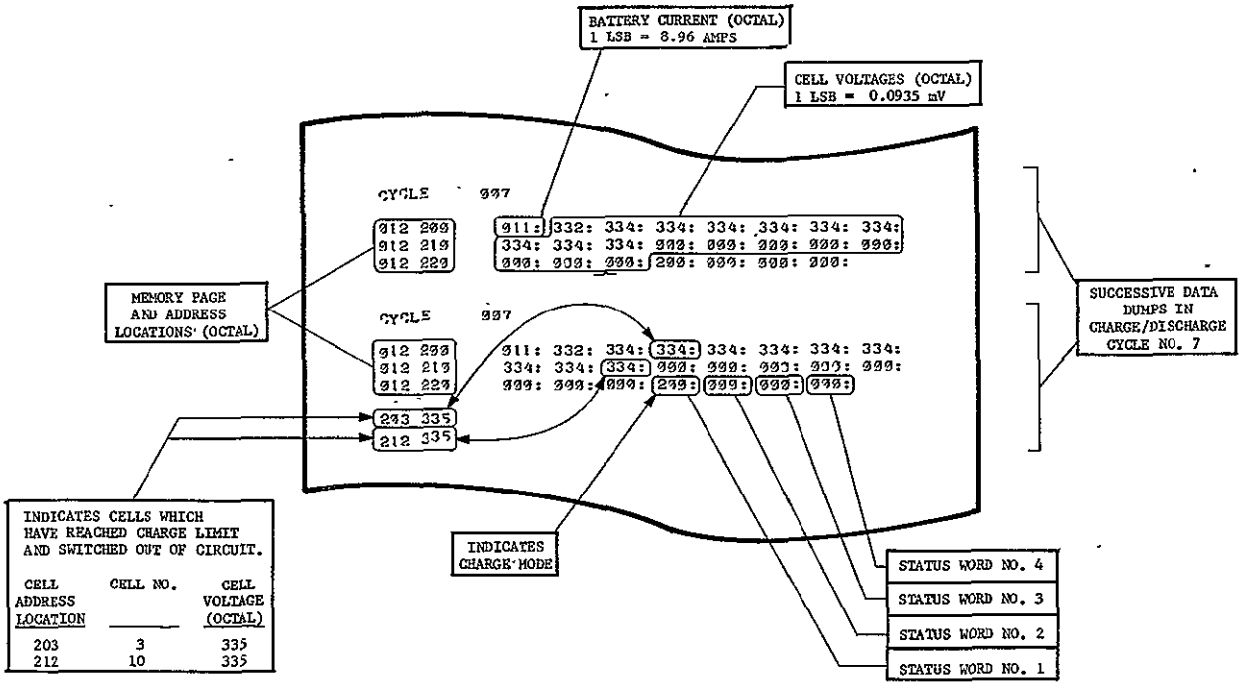


FIGURE 70 SAMPLE TELETYPE PRINTOUT

the battery must be in the charge mode. If in the discharge mode, the program will idle until a charge mode condition is obtained (Block 1). The detection of charge or discharge is made automatically in the CCP by sensing battery current. Hence, no external commands are required to cause the CCP to reconfigure all cells in circuit for a new charge or discharge half cycle. Once started in the charge mode, the CCP determines which of the 18 channels have cells connected (Block 2). Whether or not a cell is connected to a given channel is inferred from the cell voltage. If the cell voltage is zero, the CCP assumes that no cell is present and does not waste time in monitoring such cells and trying to switch them out of circuit. After determining which channels have cells

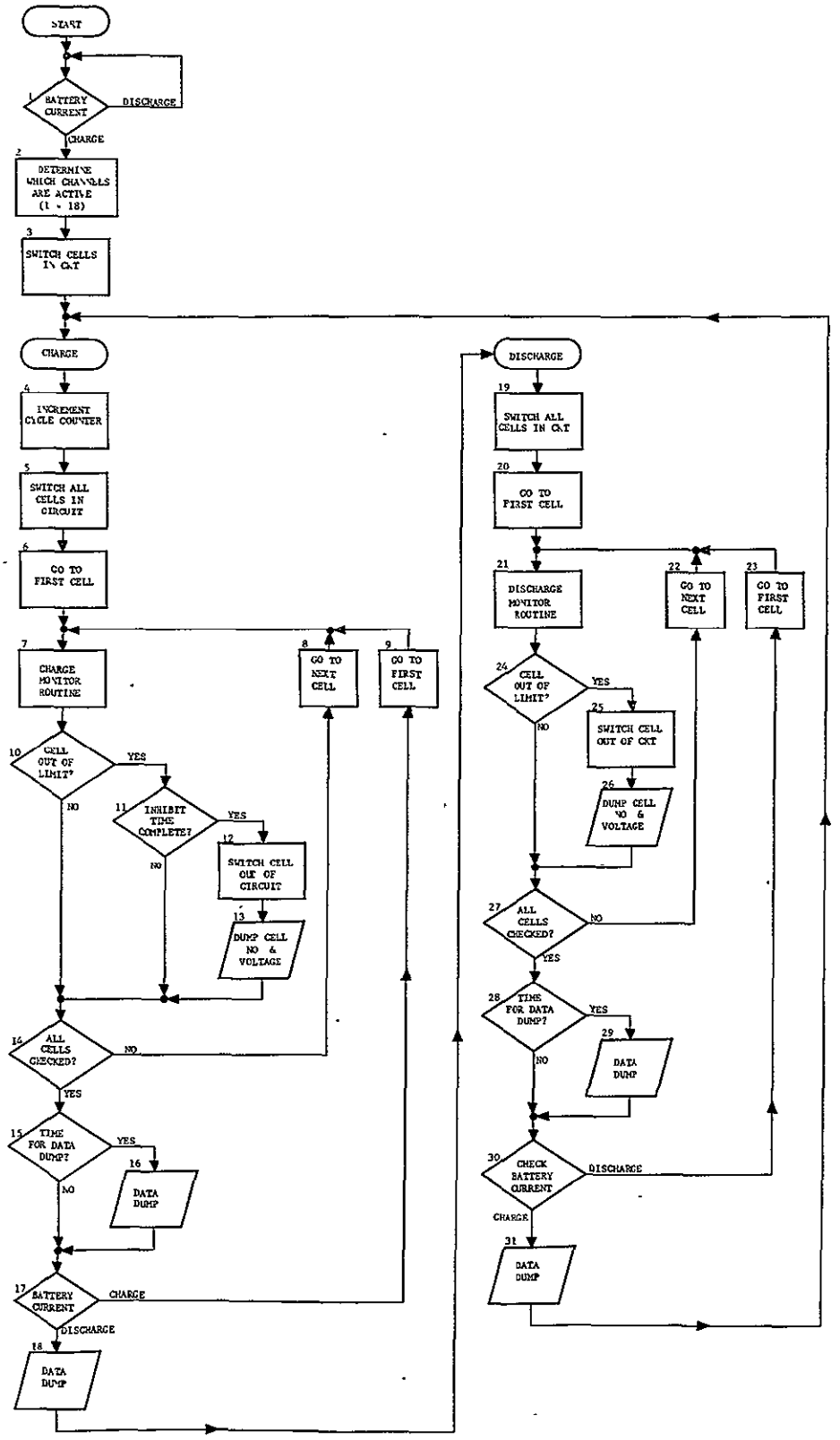


FIGURE 71. CCP SOFTWARE FLOW DIAGRAM

connected (the CCP can operate on any number of cells from 1 to 18), the CCP switches them in circuit (Block 3) and commences the CHARGE routine.

The charge/discharge cycle counter is incremented each time the CHARGE routine is entered (Block 4), all cells are switched into circuit, and the microcomputer commands the multiplexer to look at the first cell for monitoring (Block 6). If cell voltage is out of limits, the microcomputer checks to see if the inhibit time is complete; that is, whether or not the cell is out of the voltage spike region. If the inhibit time is complete, an out-of-limit indication causes the cell to be switched out of circuit (Block 12), and the cell address and voltage are printed on the teletype (Block 13). If the cell voltage is in limits, or out of limits but inhibit time is not complete, the microcomputer steps the multiplexer to the next cell (Block 8); or, if all cells have been scanned, the microcomputer checks whether it is time for a data dump (Blocks 15 and 16), dumps data if required (Block 16), then checks whether the battery is in the charge or discharge mode (Block 17). If the battery is still in the charge mode, the microcomputer commences another cell scan cycle (Block 9). If the battery has entered the discharge mode, the microcomputer commands a final data dump (Block 18) and enters the DISCHARGE routine.

Upon entering the DISCHARGE routine, all cells are switched back into circuit (Block 19), and the microcomputer commences cell monitoring at the first cell (Block 20 and 21). If a cell is out of limits, it is switched out of circuit without delay, and the cell address and voltage are output to the teletype. The scanning sequence continues (Block 22) until all cells are checked (Block 27). The microcomputer then checks whether it is time for a data dump (Block 28), dumps data if required (Block 29), and checks the battery current for charge or discharge operation. If the battery is still in the discharge mode, another cell scanning cycle is commenced (Block 23). If the battery is in the charge mode, a final data dump is made, and the microcomputer enters the charge routine.

Data dumps represented by Blocks 16 and 19 occur periodically during the charge and discharge modes. The first data dump for each mode occurs approximately 5 s after the charge or discharge routine is entered. Thereafter, a data dump occurs every 6 min for the discharge mode and every 30 min for the charge mode.

The CCP has a backup protection feature not illustrated in the flow diagram. The charge and discharge voltage limits are bounded by charge and discharge protection limits. If these are exceeded, the microcomputer will automatically disconnect the entire battery from the charging source or load by opening a master relay. Hence, if a cell bypass relay does not switch on command, the cell voltage will continue to rise or fall, as the case may be, until a backup limit is reached. The entire battery will then be open circuited in a fail-safe condition.

4.4 BREADBOARD DEMONSTRATION

The main objective of the breadboard demonstration was to show the feasibility of using the microprocessor to perform at least the same functions as the SCPs. The secondary objective was to provide some empirical data base for comparing the SCP design with the microprocessor approach.

4.4.1 System Description - The breadboard used is based on existing hardware developed in 1974 under a company-funded IR&D program for a 30-cell Ni-Cd battery. It consists of the microcomputer, command decoder, relay drivers, relay interconnection network, multiplexer, current switch network, clock, and ancillary signal conditioning circuits. The system is basically identical to the CCP conceptual design described in section 4.3.2, and will not be repeated here. The main difference is in the use of Intel 8008 SIM-8 microcomputer, which was readily available.

The following steps are performed to bring the microprocessor system into an operational state.

1) Place teletype in the ON LINE mode.

2) Push INTERRUPT button on SIM-8.

3) Place the paper tape labeled "CONSTANTS, AG-ZN, 4-6-76" in the paper tape reader. Place tape reader start/stop switch in START position. (Tape will feed in and stop when through).

4) Repeat step 3 above for the paper tape labeled "OBJECT, AG-ZN, 4-6-76".

5) Push INTERRUPT button on SIM-8.

6) Type on teletype keyboard "Ø13:ØØØ:" followed by a carriage return and line feed.

The system is now in its operating mode. If it needs to be restarted after the program has been loaded, steps 5 and 6 are performed.

4.4.2 Software Description - The software functions defined for the breadboard system are as follows:

1) Determine battery status (charge, discharge, or open circuit);

2) Determine initial system status;

3) Check all relay positions and configure them based on input data;

4) Monitor all cell voltages and charge and discharge currents;

5) Inhibit cell bypass during monoxide-to-peroxide transition period;

6) Remove the cell from series circuit whenever upper or lower limit is reached;

7) Remove charge or discharge current if cell voltage reaches an abort limit (abort limits exceed normal limits).

The detailed program flow chart (figure 4.3-11) and program description are given in section 4.3.3.

The software was developed using the Intel hardware assembler consisting of eight preprogrammed ROMs. The programmer used the ASR33 teletype to interface with the ROMs. The assembler is a two-pass system. The first pass reads the source tape and constructs a symbol table and addressing allocations. The second pass rereads the source tape and punches an object tape in octal format. This tape is loaded into read/write memory by the assembler. The octal format is then converted to the BNPF format via another program provided in the ROMs. This conversion is very time-consuming because of the low speed of the TTY. Examples of assembler formats are shown in figure 72.

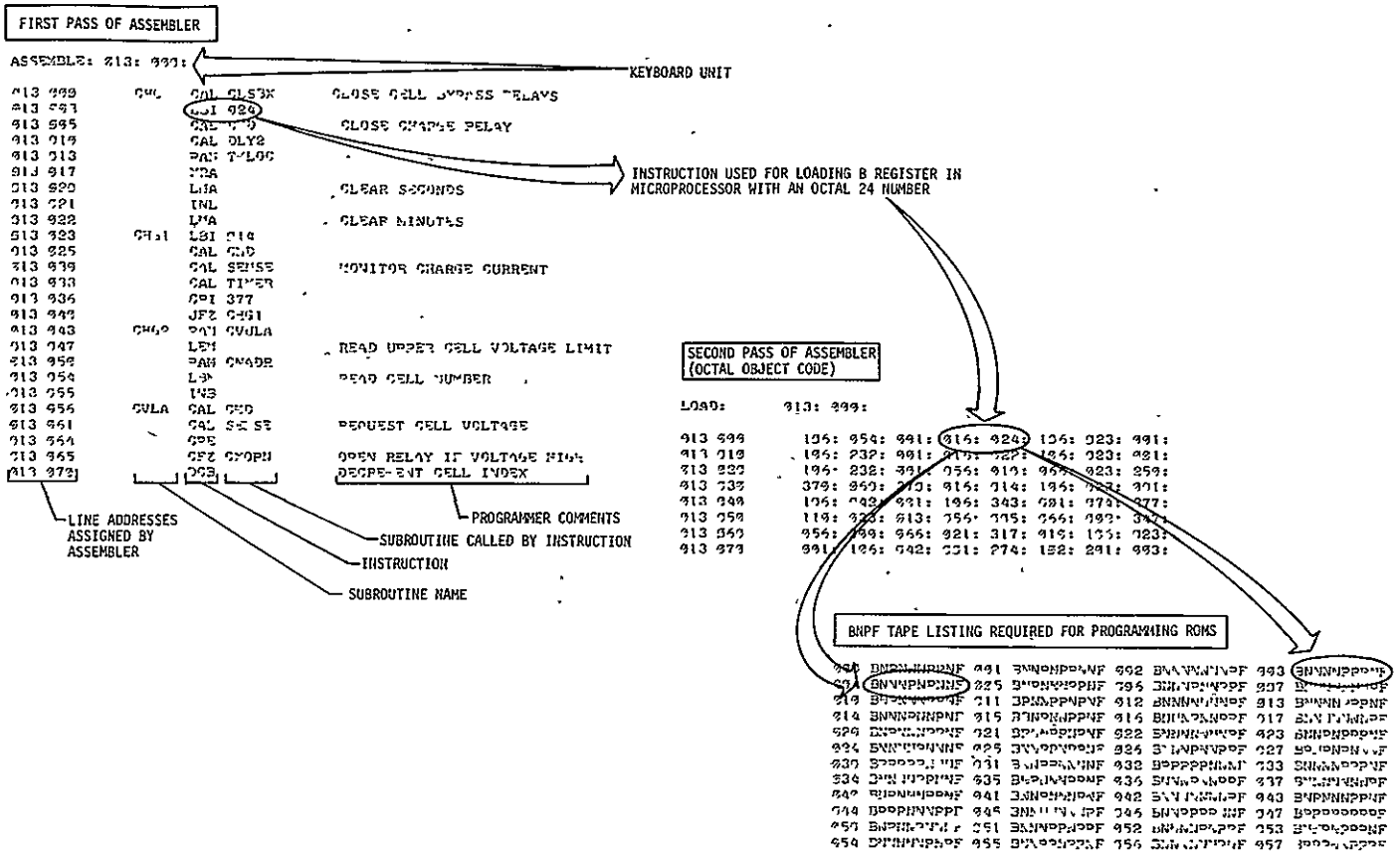


FIGURE 72 ASSEMBLER FORMATS

The software requires 1,170 8-bit memory locations. It is stored on paper tape and loaded into the RAMS when the system is initialized.

4.4.3 Test Configuration - Figure 73 shows the interface between the 10-cell battery, microprocessor control system, and ACDAS. Functions of the ACDAS were mainly to provide charge/discharge and data acquisition capabilities. Figure 74 is a photograph of the test setup.

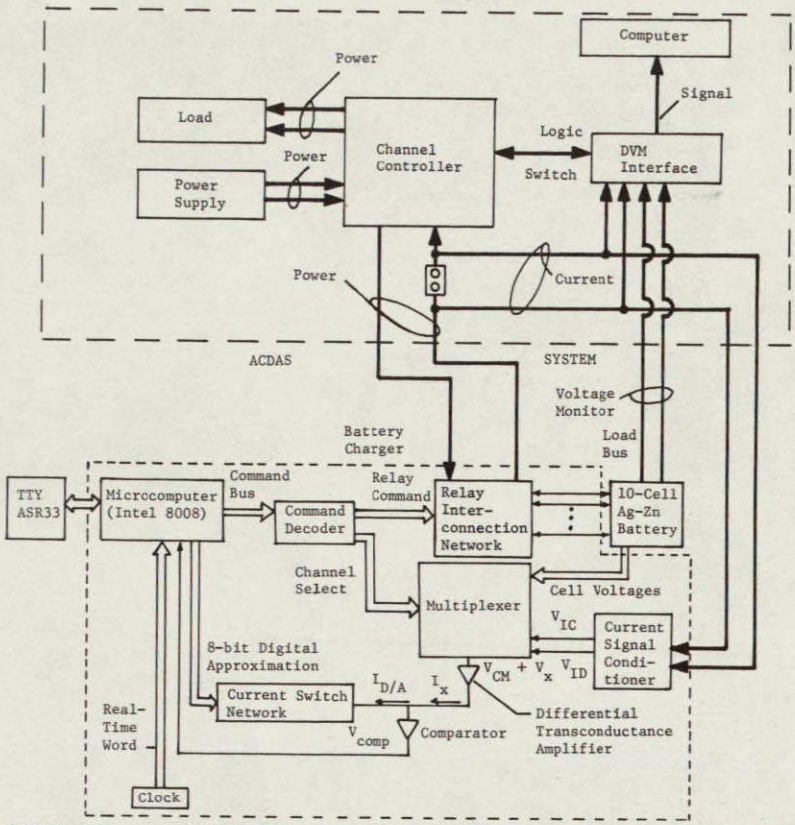


FIGURE 73 BLOCK DIAGRAM OF TEST SETUP FOR 10-CELL BATTERY UNDER MICROPROCESSOR CONTROL

4.4.4 Test Procedure - Ten cells were conditioned by charging them at the rate of 1.5 A for 30 hours, then discharging them at the rate of 6.0 A to a cell voltage of 1.250 V. This conditioning cycle was repeated twice. (No attempt was made tomatch the cells.) They were then placed in a simulated synchronous orbit under test conditions identical to those for the Group I battery in Task II.

The ACDAS controlled the orbital functions such as charge and discharge time limits. It also provided backup system protection capability and monitored and stored charge and discharge current and individual cell voltage data for verification of the microprocessor system accuracy.

4.4.5 Results and Discussion - Software was completed on January 21, 1976. Nineteen cycles of charge and discharge were completed as of April 19, 1976. During the cycles, several failures occurred that required investigation. Two basic problems occurred (1) failure of the ACDAS to supply charge and discharge current, (2) failure of field effect transistors (FETs) in the multiplexer circuit of the microprocessor control system.

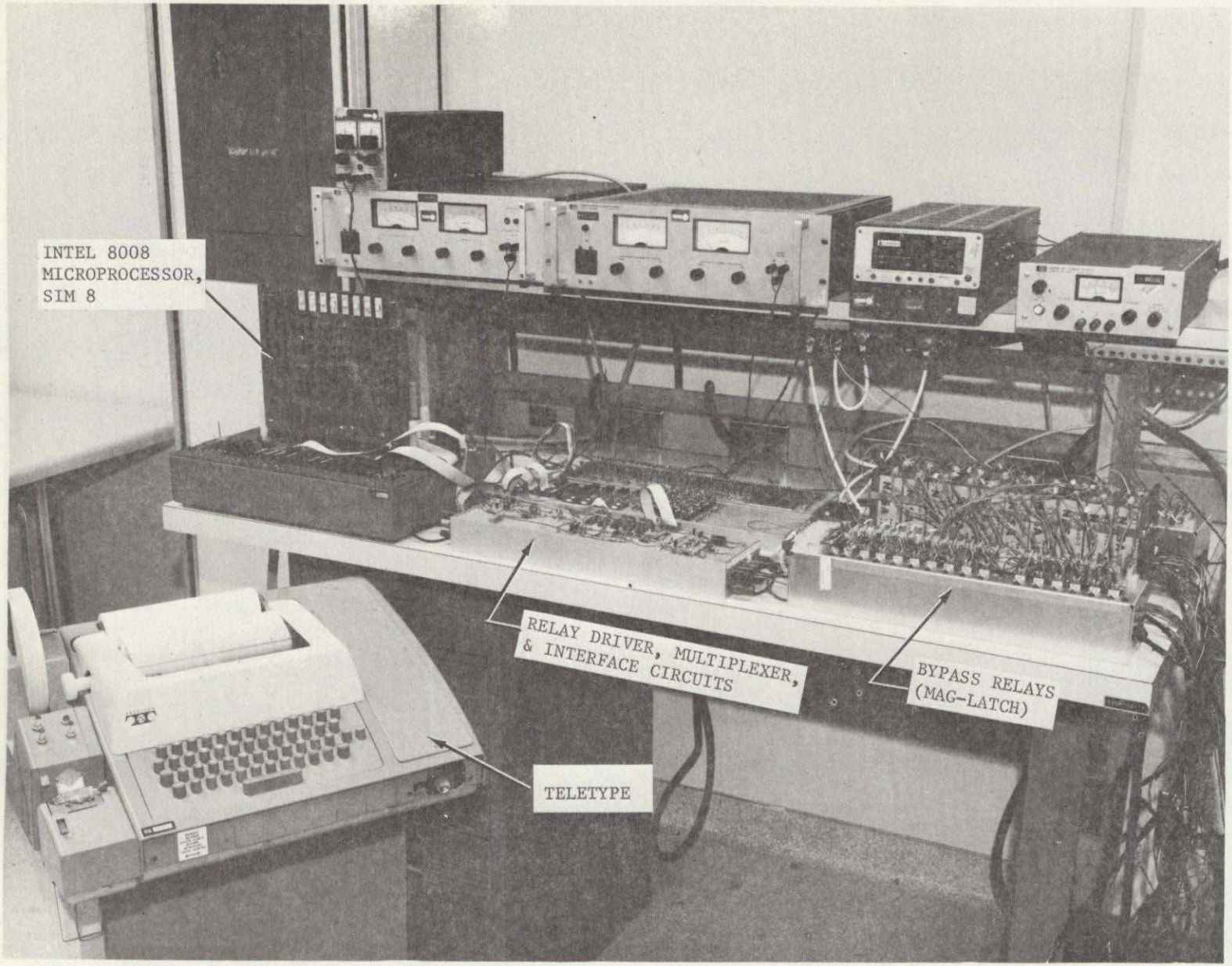


FIGURE 74 BREADBOARD MICROPROCESSOR-BASED PROTECTOR TEST SETUP FOR 10 AG-ZN CELLS

Investigation of the FET failures revealed the following.

1) All failed FETs were in a shorted mode.

2) Voltage spikes (oscillations) were being generated at the input of the FETs when the discharge current was interrupted by the switching action of the in/out cell relays. An oscillation of 4-V peak was detected when a cell was switched into the discharge circuit while discharge current was flowing.

   The main problem here was that the oscillations might at times be of sufficient amplitude (about -6.75 Vdc) to cause forward diode conduction from the input (drain) to the gate of the FET, which may have contributed to their failures.

3) There was an overlap between the turn-off of a multiplexer channel and the turn-on of the next channel. This allowed the current to flow in the FET due to common mode voltage. This condition in itself is not harmful if the FET is functioning normally. A good FET limits this current to the saturation current $\left(I_{dss}\right)$. However, if the FET has been damaged, for instance from over-reverse voltage, the current might not limit to I_{dss}. In this case, shorting of gate to source can occur with source to drain shorting and then burn open.

The oscillation problem was resolved by a software change that ensures that no cell in our relays is switched in while current is flowing. The turn-on overlap problem was solved by a software change that ensures a 2-ms delay between a channel turn-off and turn-on of the next channel.

Test data obtained during the first 19 cycles yielded results very similar to those for the Group I battery. Testing will be continued during Phase II of this contract, and its results will be included in the Phase II final report.

The significant results of the breadboard demonstration are as follows.

1) It provides a very significant flexibility in charge control. Selection of control techniques can be at the battery or cell level, and various charge modes can be selected. Because only firmware (programmed ROM) changes are necessary, no hardware modifications are needed to provide the charge control flexibility.

2) It can monitor system and individual cell parameters and transmit these data to a central data acquisition system.

The major development required in the use of a microcomputer is in the software. Two problems are associated with the software. These are:

1) Assembly language must be used in writing the program. A higher level language PL/M, is available for the Intel 8080 System, but its use incurs significant cost. This results in a tradeoff between software development cost using assembly language and possible lower software development time and cost via PL/M language.

2) Software preparation and debugging represent a significant portion of the total development effort in the microprocessor-based design. Difficulty encountered with the software development depends on the programmer's familiarity with the particular machine with which he is working.

4.5 COMPARISON OF BATTERY PROTECTION APPROACHES

One objective of Task III was to comparatively evaluate the SCP with the microprocessor-based design, then recommend a preferred approach to protect the AG-Zn battery. To perform the evaluation, the following data base was developed and considered.

1) Detailed conceptual design of microprocessor-based design (referred to as Computer-Based Cell Protector, CCP, and described in paragraph 4.3)--the design was developed to a degree that will permit a realistic comparison with the SCP.

2) Comparative data on SCP and CCP.

3) Test data and operating experience on a breadboard CCP with a 10-cell Ag-Zn battery. The results of breadbaord demonstration are presented in paragraph 4.4.

Design factors defined for the two approaches are cost, performance, reliablility, weight, size, power consumption, and control flexibility. Comparison of these factors is summarized in Table 12. Tables 13 and 14 show the detailed list of parts and hardware cost for the SCP and CCP, respectively. The conceptual packaging configuration for the CCP is illustrated in figure 75. Piece part reliability estimates of the two design approaches were made. Appendix B provides the details of this reliability analysis.

TABLE 12. COMPARISON OF SCP AND CCP DESIGN APPROACHES FOR 18-CELL AG-ZN BATTERY

Parameter	SCP	CCP
Material Cost	$38.99 ($213 per SCP)	$2,827.12
Performance		
Charge control flexibility	Limited to simple charge control technique (i.e., voltage cutoff) Cutoff voltage limit adjustment done manually & very difficult	Various techniques can be implemented via software (e.g., ampere-hour recharge fraction, multiple voltage limits, & modified constant current). Voltage limit adjustment made via TTY; relatively simple
Cell voltage monitoring	Limited to hardwired connection to cell terminals	Capability to store all measured parameters & dump data on output device such as teletype whenever required.
Application flexibility	Modular design; well suited to single-cell applications	Integrated design; best suited for full battery application
Power consumption	6.5 (360 mW per SCP)	2.5 W
Reliability		
Success probability for 1 year	0.943	0.974
Success probability for 2 years	0.889	0.949
MTBF	148,000 hours	331,000 hours

TABLE 12. (CONCLUDED)

Parameter	SCP	CCP
Design		
No electronic piece parts	1378	398
Circuit board area	1684 cm^2 (93.55 cm^2/SCP)	477.4 cm^2
Volume	82.6 cm^2	209.3 cm^3
Weight	4.73 kg (263 gm/SCP)	2.82 kg
Interface		
No. of power & signal wires	162	58
With data handling system (DHS)	Hardwired connection required, resulting in complex wiring; Requires A-to-D conversion in DHS	Minimum required because CCP operates in digital formal

TABLE 13 SCP PARTS LIST

Description	Quantity	Estimated Part Cost, $
Switch nonlatching, MSS-22	1	1.17
1C dual in-line op amp, LM324N	2	2.50
1C dual in-line, MC14020CP	2	3.33
1C dual in-line, MC14001	1	0.42
1C dual in-line, MC14011	1	0.42
Relay 25-A magn latching, KCL-D2A-002	1	77.00
Diode, 1N4148	8	.22
Diode, 1N458	2	.47
Diode unitrode, JAN 1N5550	1	1.32
Zener diode, 1N5257B	1	.93
Zener diode, 1N4566	1	11.70
Transistor, field effect, 2N5392	3	5.00
Transistor, 2N2907A	3	.91
Transistor, 2N2222A	5	.27
Transistor, 2N3019	1	1.50
Resistor, variable, 3006P-1-103	2	1.19
Resistor, 10 KΩ	3	.28
Resistor, 1 KΩ	2	.44
Resistor, 2.15 KΩ	1	.44
Resistor, select in test	2	.44
Resistor, 2.87 KΩ	1	.44
Resistor, 7.5 KΩ	1	.44
Resistor, 10 MΩ	3	.28
Resistor, 2.2 MΩ	4	.28
Resistor, 750 KΩ	2	.28
Resistor, 110 KΩ	1	.44
Resistor, 10 KΩ	1	.44
Resistor, 13.3 KΩ	1	.44
Resistor, 2.61 KΩ	1	.44
Resistor, 51 KΩ	3	.28
Resistor, 5.1 KΩ	2	.28
Resistor, 100 KΩ	2	.28
Resistor, 300 KΩ	1	.28
Resistor, 20 KΩ	1	.28
Capacitor, 15 µF	1	.70
Capacitor, 0.1 µF	4	.57
Connector, receptacle	2	5.50
Connector, plug	2	6.84
Case & cover	1	44.34
Printed circuit boards (recurring cost)	3	65.00*
Total per SCP:	77	$213.00
Total 18 SCPs:	1386	$3899.00

*Recurring

TABLE 14 CCP PARTS LIST

Description	Quantity	Estimated cost, $
Multiplexer		
2N5392 N-channel FET	96	480.00
Resistor, 1 mΩ 5%	48	7.00
8-Channel differential		
D125BK 6-channel FET-switch driver	1	8.50
100 KΩ, 5% resistor	6	0.84
1N4148 diode	1	0.19
Subtotal	152	496.53
Relay Driver		
MC14628 Binary-to-octal decoder	2	4.00
2N2222 NPN transistor	22	22.00
2N2907	6	6.00
5 KΩ 5% 1/2-W resistor	14	2.10
2 KΩ 5% 1/2-W resistor	14	2.10
1.8 KΩ 5% 1-W resistor	6	1.00
Subtotal	64	37.20
Relay Interface		
Relay, latching 25 A	18	1396.00
1N4148 diode	72	13.46
1N5550 diode	18	22.86
Subtotal	108	1432.32
Transconductance Amplifier		
LH0004CH high-voltage operational Amplifier	2	70.20
2N3811 dual PNP transistor	1	1.00
1N4148 diode	7	1.30
10 KΩ resistor 5%	2	0.30
390 KΩ resistor 5%	1	0.15
Select 1% resistor	1	0.15
100, 47, 300, 510 pF capacitor	4	4.00
Subtotal	18	77.10
Current Switch Network & Comparator		
LM324 quad operational amplifier	1	3.75
LM111 voltage comparator	1	4.85
2N2907 PNP transistor	1	1.00
1N4148 diode	3	0.56
1N4566A 6.4-V zener	1	12.00
ICL8018 quad current switch	1	3.30
ICL8018 quad current switch	1	3.30
Resistor, 5%	4	0.60
Resistor, 1%	10	1.00
Resistor, ladder network	2	50.00
4.7 μF capacitor	2	2.00
0.1 μF capacitor	3	3.00
3300 pF capacitor	1	1.00
Subtotal	31	86.35
Signal Conditioner		
LM324 quad operational amplifier	1	3.75
Resistor select, 1%	5	0.50
1 KΩ, 1% resistor	2	0.20
Subtotal	8	4.45
Microcomputer		
Intel 8080 microprocessor	1	175.00
MC14508 dual 4-bit latch	5	32.50
MC14081 AND gate qual 2 input	2	2.00
MC14011 NAND gate qual 2 input	2	2.00
MC14020 14-stage counter	2	6.66
1 Crystal	1	10.00
Intel 5101 256X4 static RAM	2	60.00
Intel 8702 256X8 PROM	1	40.00
Clock generator & driver for 8080	1	65.00
Subtotal	17	393.16
Miscellaneous (connectors, case & cover)		
Connector, case & cover	3	200.00
Printed circuit board	2	100.00
Total:	403	$2827.12

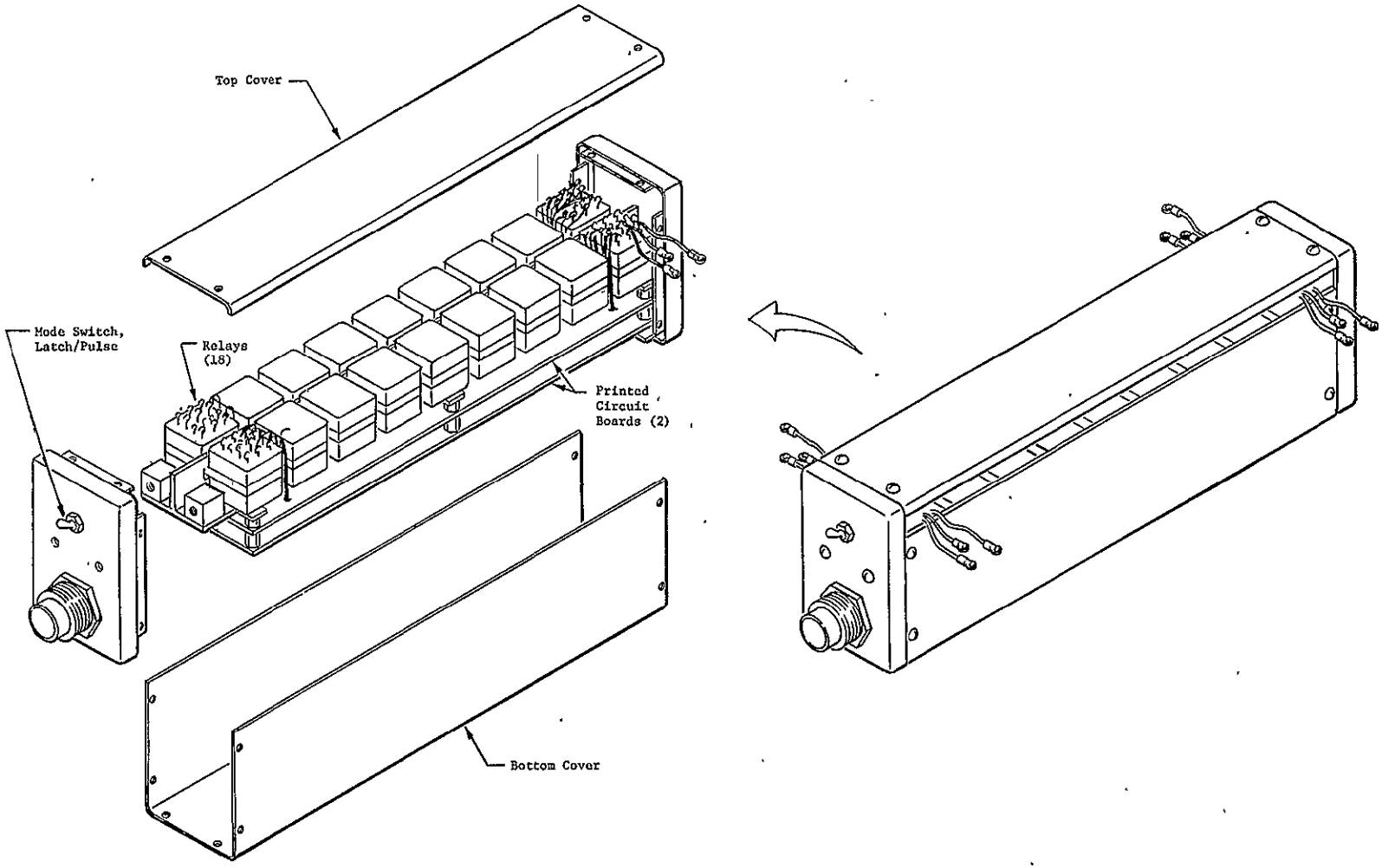


FIGURE 75. CCP PACKAGING CONFIGURATION

The main advantages of the SCP design relative to the CCP approach are:

1) It is a modular design and better suited for single cell applications;

2) No software is involved;

3) The analog circuits are straightforward and relatively simple.

Advantages of the CCP approach range from cost factors to reliability, interface and application flexibility, as indicated in table 12. The major disadvantage is that it involves the software and requires a specially trained person to prepare the computer program. In the case of Intel 8008 (SIM 8), the program was written in assembly language and loaded into the RAM.

After a careful evaluation of the advantages and disadvantages, it was concluded that no single approach can staisfy all applications. The CCP approach is better suited for the 18-cell battery where (1) flexibility in changing the charge control limits or conditions are required and (2) both volume and weight must be minimized.

5.0 CONCLUSIONS AND RECOMMENDATIONS

Single cell protectors (SCPs), each housed in a separate assembly, have been designed and fabricated for use on one or more rechargeable Ag-Zn cells operating in series. During this Phase I contract period, eighteen SCPs have successfully provided individual cell protection for an 18-cell battery pack.

Based on initial 100 cycles of simulated synchronous orbit performed (as of April 18, 1976), at 40% depth of discharge and at 22°C, no significant differences exist between cell-level control and battery-level protection and control. Preliminary conclusions on the evaluation of cell-level and battery-level protection approaches are that 1) the cells have demonstrated good performance uniformity such that individual cell bypass capability is not yet necessary and 2) the selected upper charge voltage limit of (1.98 Vdc per cell) 35.64 Vdc for the battery-level control pack prevents internal cell pressure buildup and thus provides adequate overcharge protection.

The best method of providing control and protection of the Ag-Zn cells is dependent on the specific application. For laboratory use involving a large number of cells and batteries, the microprocessor concept provides a low-cost approach with high flexibility in charge control adjustment combined with data acquisition capability. On the other hand, the SCP with its simplicity in construction and attachment to one or more cells is best suited for testing a limited number of cells or batteries. The SCPs are also suitable for spacecraft application if their volume and weight requirements can be tolerated.

APPENDIX A

AUTOMATIC CONTROL AND DATA ACQUISITION SYSTEM (ACDAS)

The ACDAS is a fully automated fail-safe system that remotely controls individual cells and batteries through specific cycles and acquires test data in a readily reducible form for analysis. An overall view of the control equipment is shown in figure A-1.

An operating fuctional diagram of the ACDAS is shown in figure A-2. Two PDP 8-8K memory computers are the heart of the system. Each computer performs all functions, thereby ensuring that 50% of the equipment will be operating at all times in case of a computer breakdown.

Twenty-one test channels are available that permit 21 individual cycle profiles to be performed instantaneously. Each channel has four voltage and current phases that permit a cycle profile to have four individual power levels. In addition, each channel is capable of operating up to 100 V and 100 A on each phase.

The system has a 900-cell control operating capability.

Individual phase and cell control is achieved by programming control limits into the computer. The computer monitors individual cell data, compares the data with the control limit, and terminates the phase for that particular cell when one of the limits is attained. The cell will then be switched to the next operating phase. Each phase may be controlled by any three of the following control parameters: (1) number of cycles, (2) cell or battery voltage, (3) current, (4) third electrode signal or equivalent, (5) pressure, (6) temperature, and (7) time.

In addition, battery test control may use individual cell data in the battery. For example, the test may require that no individual cell fall below 0.5 V on discharge. The battery could be controlled on this basis.

Data acquisition is accomplished by a crossbar scanner and digital voltmeter capable of measuring dc voltages to 10 μV. All data are recorded on magnetic tape and teletype for direct printout when necessary.

Software programs using the Martin Marietta CDC 6500 computer reduce and analyze the data stored on the ACDAS magnetic tape. Present programs are capable of the following tasks:

1) Strip data into individual channels;

2) Isolate specific data or cells for individual evaluation;

3) Statistically evaluate performance parameters of groups of cells or batteries;

4) Provide call matching and selection.

Data are stored on a master tape and are available on magnetic tape, microfilm, X-Y plots, and computer printout.

Support equipment housing the cells and batteries comprise ten 27-ft^3 temperature chambers with a temperature range of -120°F to +360°F. Two of these chambers include a nitrogen source for heat sterilization of component parts. Figure A-3 shows some of this equipment.

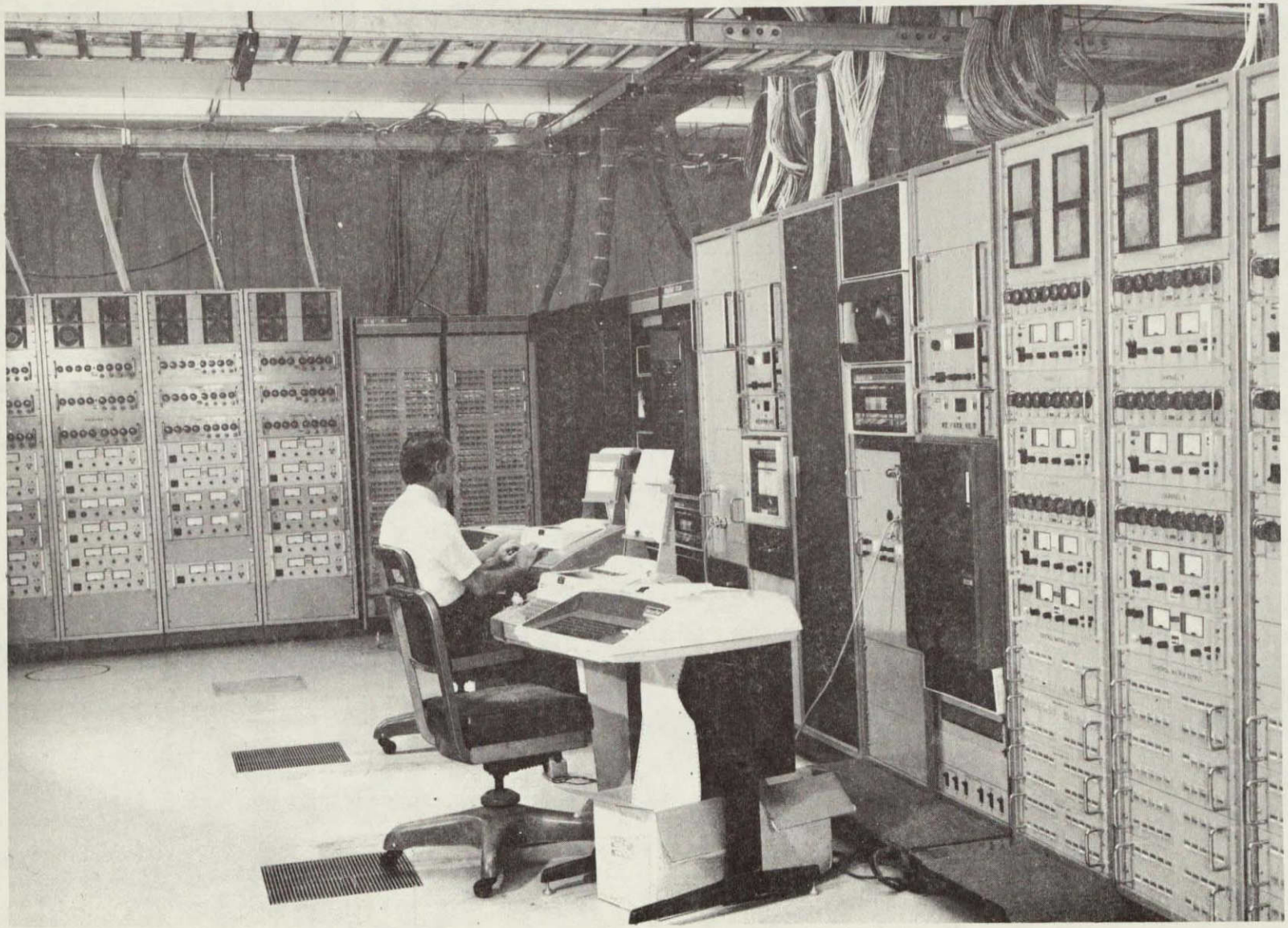


FIGURE A-1 AUTOMATIC CONTROL AND DATA ACQUISITION SYSTEM

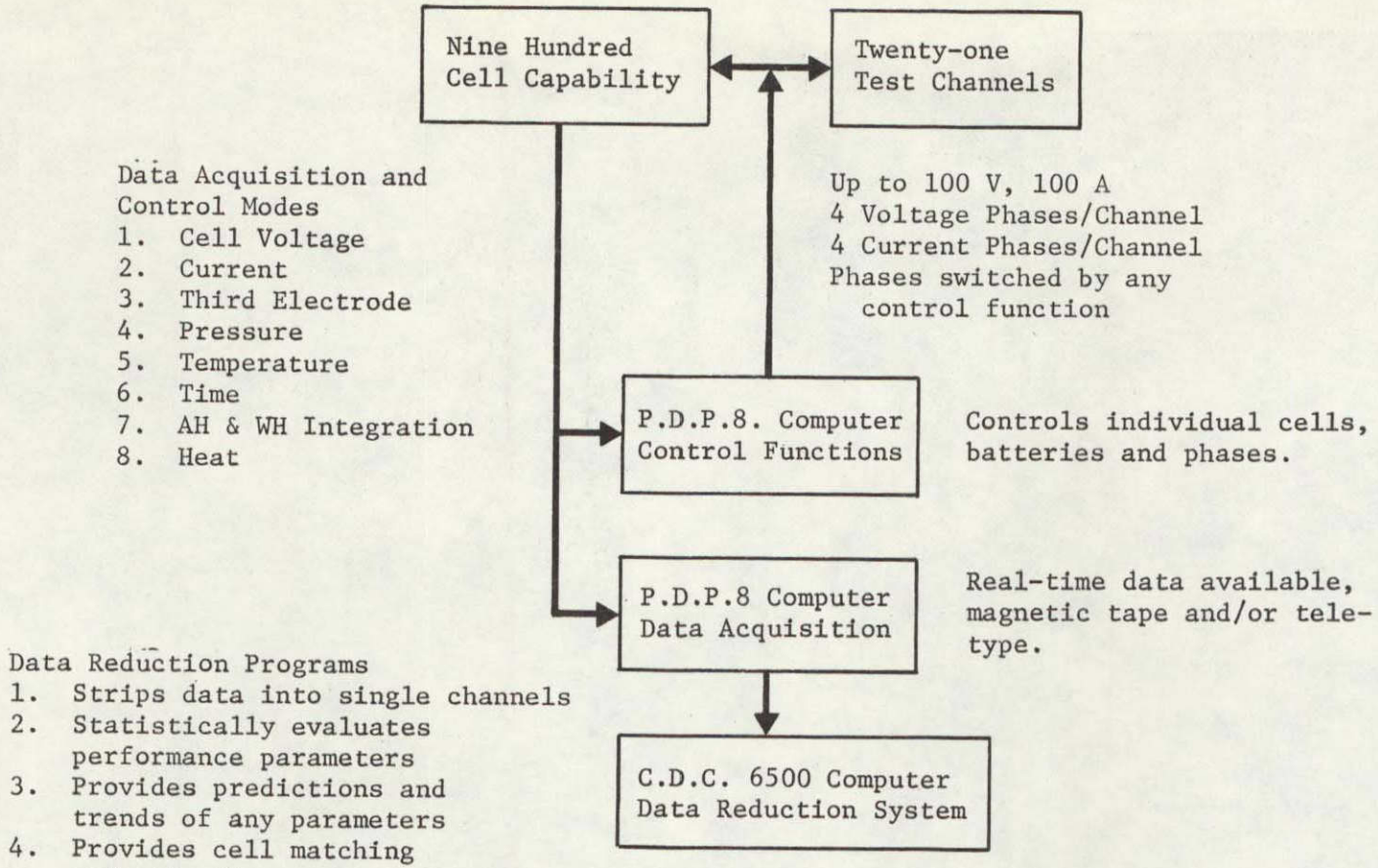


FIGURE A-2 ACDAS FUNCTIONAL BLOCK DIAGRAM

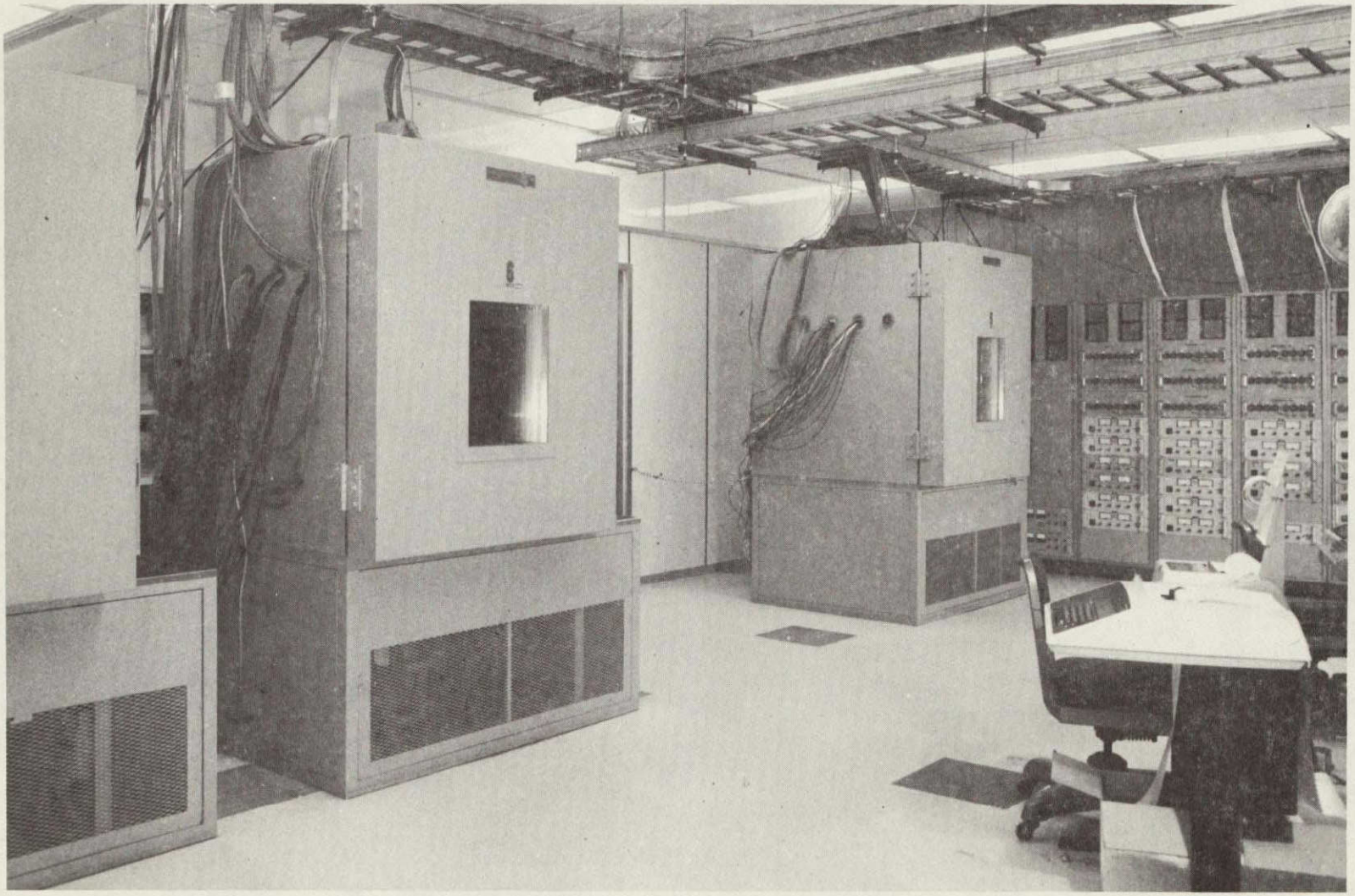


FIGURE A-3 THERMAL CHAMBERS FOR BATTERY TESTS

APPENDIX B - RELIABILITY ANALYSIS

A reliability analysis was conducted to compare four of the basic configurations under consideration. Procedures and data of MIL-HDBK-217B, 217B, *Reliability Prediction of Electronic Equipment,* were used to estimate the probabilities that the denoted charge and battery protection systems will maintain each cell of an 18-cell battery within specified voltage limits for a specified period of time (success).

Conclusions and Recommendations - Estimated probabilities of success for 1 and 2 years of continuous spatial operation are shown in table B-1. The electronic parts count of each configuration is included for comparison.

TABLE B-1 PROBABILITIES OF SUCCESS FOR OPERATING ONE BATTERY

Configuration	Parts count	Success probability	
		1 Year	2 Years
SCP	1314	0.943	00.889
CCP	401	0.974	0.949

The CCP design has the lower piece part count and the higher reliability. Because of a higher parts count, the SCP has the lower reliability. The reliability of the CCP could be enhanced by either reducing the number of FETs or employing redundancies of FETs. If feasible, making the FETs completely redundant would increase the 1-year probability of success for the CCP.

The electromechanical relays also greatly contribute to total failure probabilities. Table B-2 presents failure probabilities for generic categories for each configuration considered. Solid-state switches, which have higher reliability than relays, cannot be used in this application because of their high voltage-drop characteristics.

TABLE B-2 FAILURE PROBABILITIES BY GENERIC PART CATEGORY AND MTBF

Piece part	Failure probability, ppm/hr	
	SCP	CCP
Relay	0.3150	0.3150
FETs	0.7801	1.5503
Resistors	0.1900	0.0457
Transistors (non-FET)	1.0410	0.1346
Diodes	0.4102	0.0352
ICs	3.2400	0.7500
Capacitors	0.3901	0.0540
Connectors	0.3600	0.0600
Crystal	--	0.0100
Substrate	--	--
Other	0.0236	0.0600
Total	6.7500	3.0148
MTBF	148,000 hr	331,000 hr

Approach - Reliabilities of the four configurations were estimated using the parts count by generic category and generic failure rates modified by environmental and quality level factors. MIL-HDBK-217B provided the general approach and data. Basic assumptions concerning the parts were:

1) Satellite benign environment;

2) Average temperature of 25°C;

3) All parts must function for success;

4) JAN TX parts quality;

5) Class A parts screening;

6) Part deratings in general agreement with NASA practice:

Resistors - 60% of rating

Transistors - 70% of rating

Diodes - 70% of rating

Relays - 60% of rating

Switches - 70% of rating

Capacitors - 60% of rating

7) Average resistor tolerance = 10% unless otherwise noted in parts list;

8) Average chip area = 4900/sq mils;

9) Thick film networks used in hybrid;

10) Conductor density = 66/in.^{2};

11) Gold wires and eutectic bonding employed;

12) Three mat etch cycles used;

13) Equipment operates continuously.

Operating in-service failure rates for each generic part category were calculated using the general relationship for nonhybrids:

$$\lambda_p = \lambda_b \left(\Pi_E \times \Pi_A \quad \Pi_{S2} \times \Pi_C \times \Pi_Q\right) \qquad [B1]$$

where: λ_p = part failure rate, ppm/hr

λ_b = base part failure rate, ppm/hr

Π_E = environmental factors other than temperature

Π_A = application factor

Π_{S2} = voltage stress factor

Π_C = construction class factor

Π_Q = quality level factor

For example, the failure rate of an RCR05, 10-kΩ resistor (MIL-R-39008) is calculated as shown below:

Per MIL-HDBK-217B, tables 2.5.1-1 through 2.5.1-4.

λ_b = 0.0004 ppm/hr (derated 40%, @ 25°C)

Π_E = 1.0 (satellite, S_F)

Π_R = 1.0 (up to 100K)

Π_Q = 0.3 (level P)

$$\lambda_p = \Pi_b \Pi_E \Pi_R \Pi_Q \qquad [B2]$$

λ_p = (0.0004) (1.0) (1.0) (0.3) = 0.00012 ppm/hr each.

This type of calculation is performed for all resistors and the failure rates added to obtain the total failure rate for all resistors. As listed in table B-2, the total resistor failure rate for the SCP is 0.1900 ppm/hr. The procedure for the resistors is repeated for all generic categories of parts. Their sum (no redundancies) equals the total failure rate of a particular configuration--6.75 ppm/hr for the SCP (table B-2).

The success probability for 1 year of continuous operation is calculated by the equation

$$P(S) = \exp\left(-\lambda_p t\right) \qquad [B3]$$

where:

P(S) = success probability for one year

λ_p = sum of part failure rates for configuration

t = operating hours = 8760

Hence, the 1-year success probability for the SCP configuration is:

$$P(S) = e^{-(6.75)\ (8760)\ (10^{-6})} = e^{-0.05913}$$

$$= 0.94258$$

The Martin Marietta-derived average failure rate of 0.030 x 10^{-6}/hr was used for all ICs rather than perform laborious calculations for each type of IC. This value is for achieved operating, hi-rel ICs. Industry and government surveys by Martin Marietta plus our comparative studies proved this to be a good average value (ref: *Handbook of Piece Part Failure Rates*, Martin Marietta Corporation, Denver Division, T-70-48891-007).